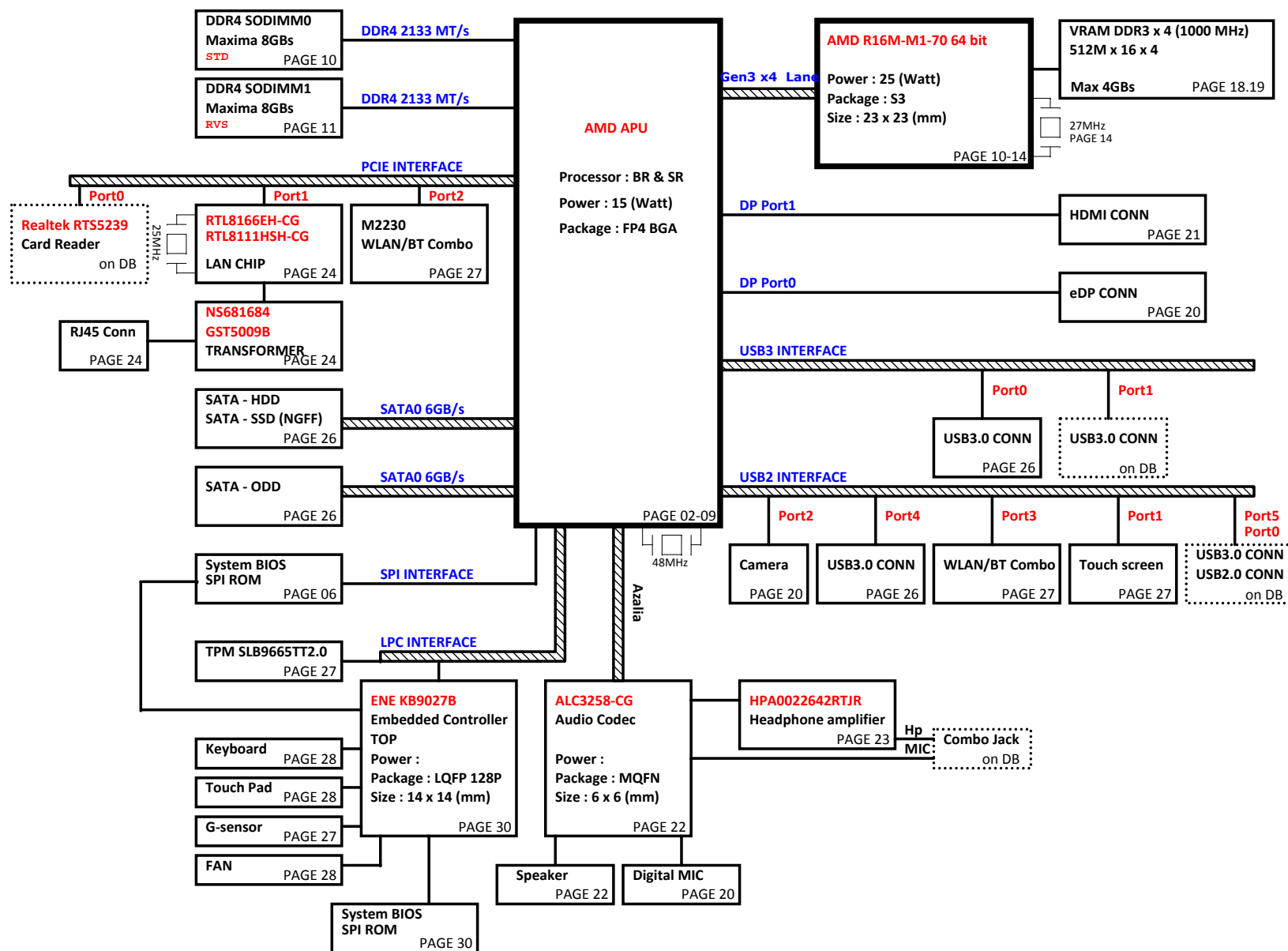


Dessert AMD BR & SR DIS/UMA 15.6"



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

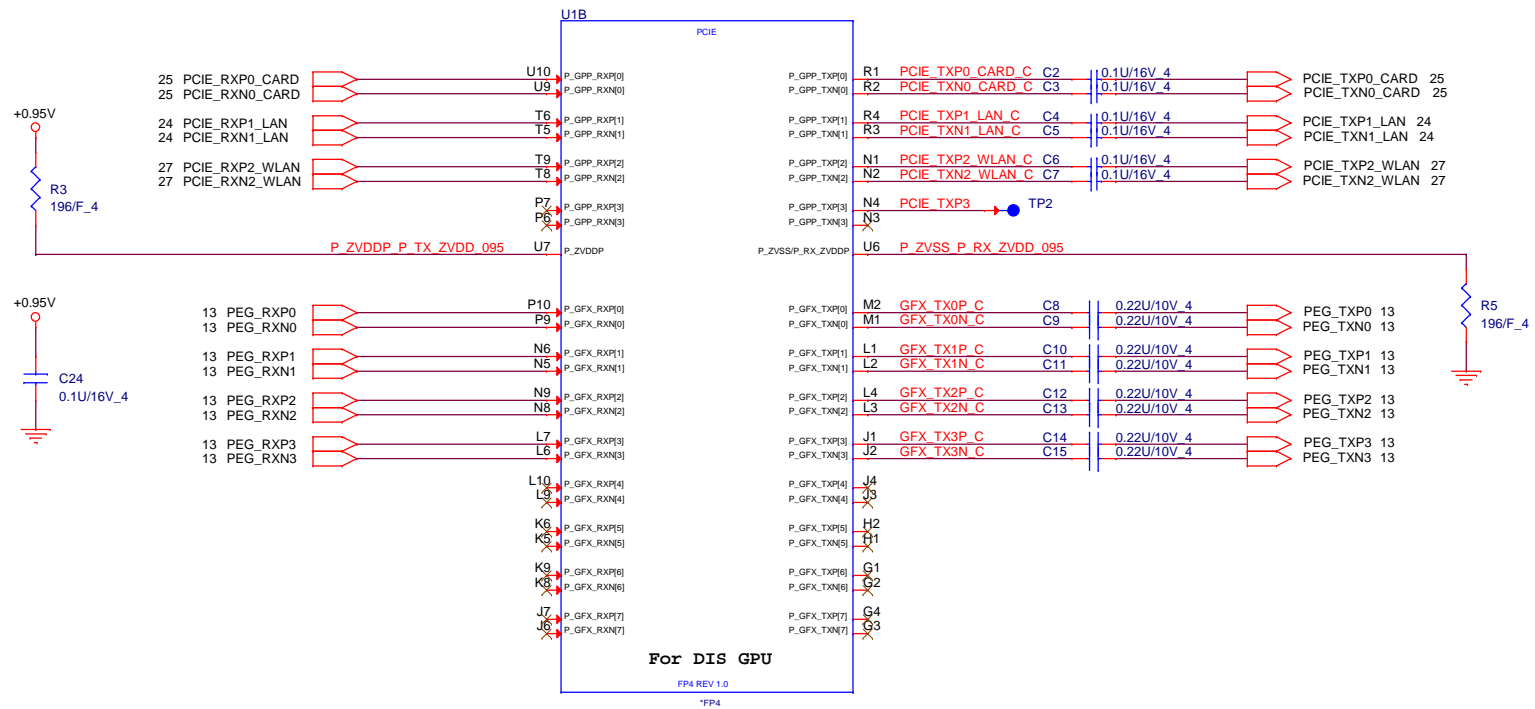
Power Source

ISL88750 System Charge Power (+BATCHG) PAGE 31
SY8208B/SY8286C System Power (+3VPCU/+5VPCU/+3VS5/+5VS5) PAGE 32
RT8231B System Memory Power (+1.2VSUS/+0.6V_DDR_VTT/+2.5VSUS) PAGE 33
APW8826/APW8826/G9336 Processor Power (+0.95VS5/1.5VS5/0.77VS5) PAGE 34
AO21267/RT8068AZQW Processor Power (+0.95V/+1.8VS5) PAGE 35
ISL62771 Processor Power (+VCC_CORE/+VDDNB_CORE) PAGE 36.37
ISL62771 Processor Power (+APU_VDDGFX) PAGE 38.39
APL3523A *3 System Power (+3/+3VLAVCC/+5V/+3VSUS/ +1.5V/+1.8V_ROM/+1.8V) PAGE 40
G5018 Processor Power (+VDDCR_FCH_S5) PAGE 41
RT3662EB/AO21236 DGPU Power (+VGA_CORE/+1.35V_VGA) PAGE 42~44
RT8068A/APL3523A DGPU Power (+0.95V_VGA/+3V_VGA/+1.8V_VGA) PAGE 45



PROJECT : G54A
Quanta Computer Inc.

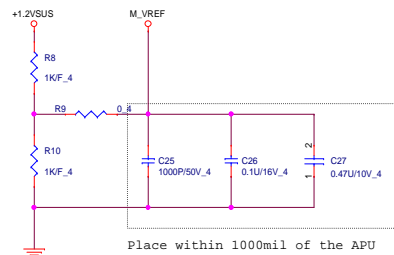
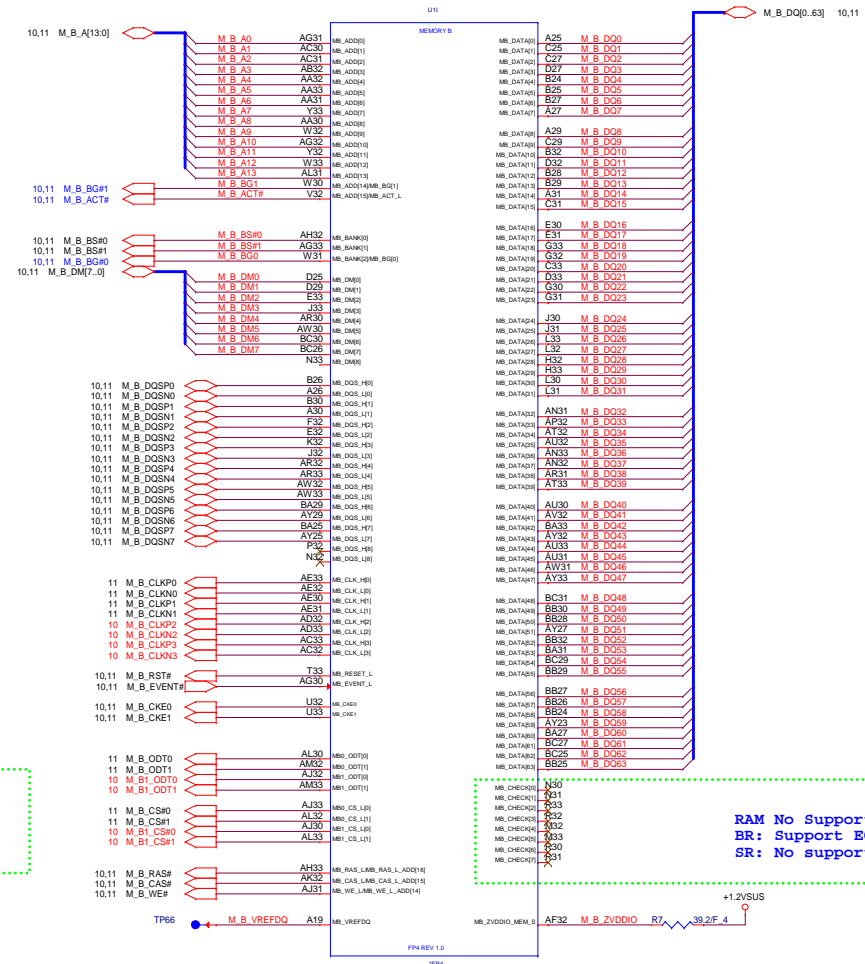
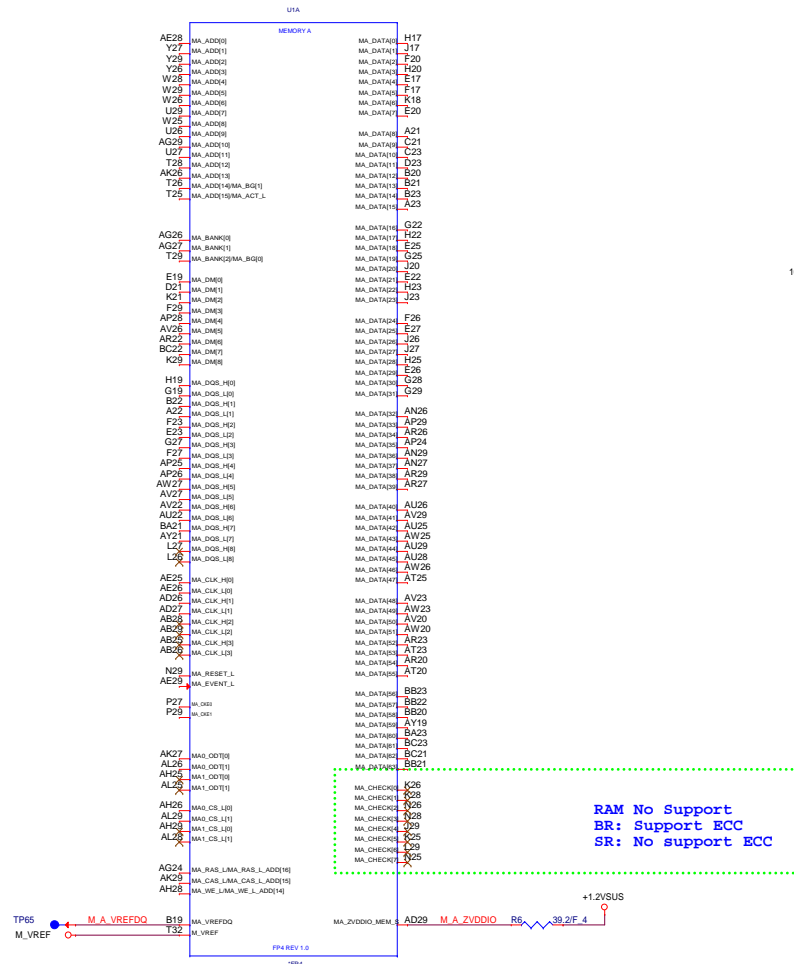
Size	Document Number	Rev
	Block Diagram	1A
Date: Monday, January 11, 2016	Sheet	1 of 46



PROJECT : G54A
Quanta Computer Inc.

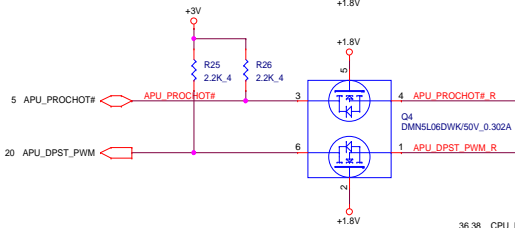
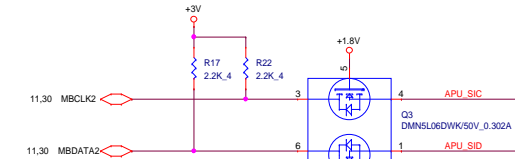
Size	Document Number	Rev
	BR & SR 1/7(PCIE)	1A
Date: Monday, January 11, 2016	Sheet 2 of 46	

SB only channel B

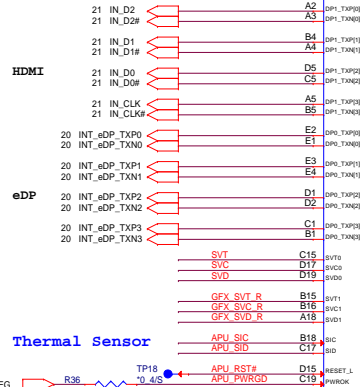
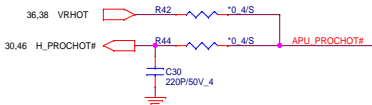


```
RAM No Support
BR: Support ECC
SR: No support ECC
```

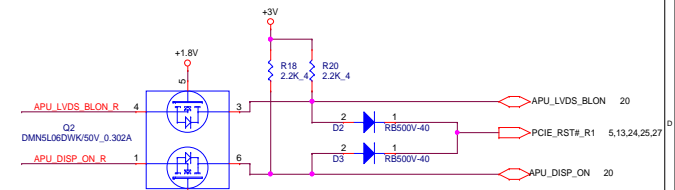
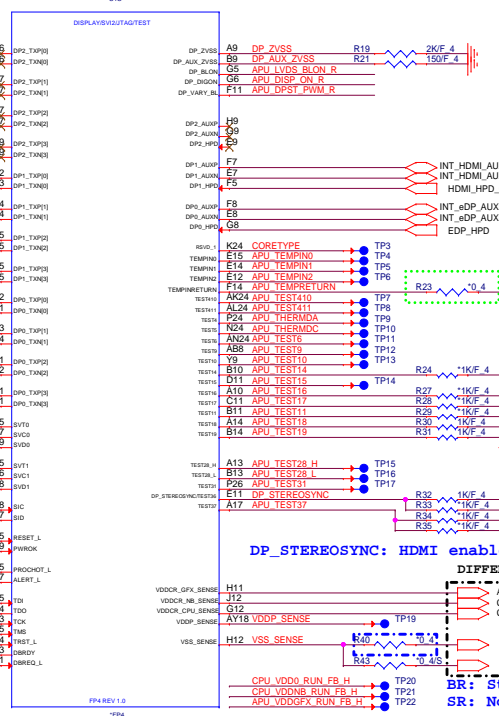
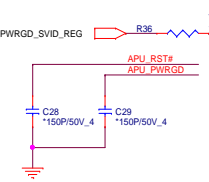
```
RAM No Support
BR: Support ECC
SR: No support ECC
```



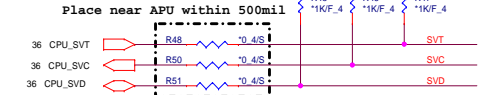
EC H_PROCHOT#



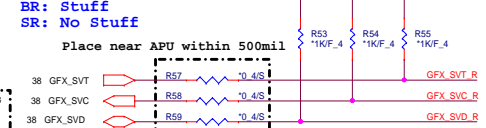
Thermal Sensor



APU Serial VID

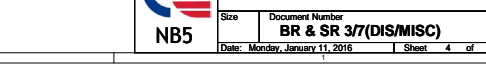
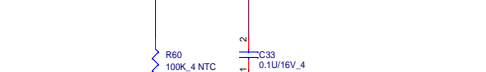
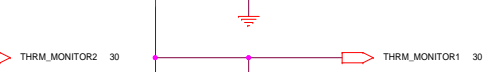
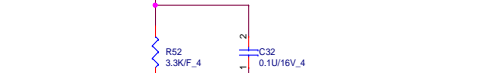


GFX Serial VID



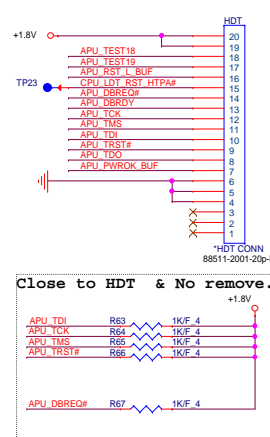
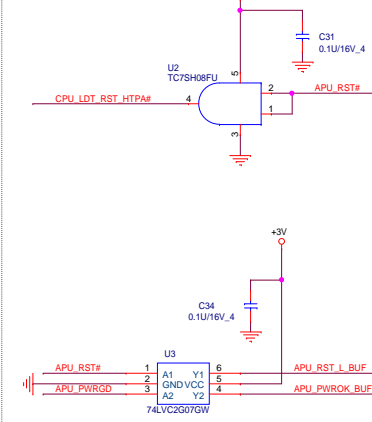
BR: Stuff
SR: No Stuff

Place near APU within 500mil

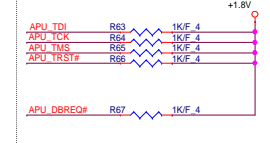


HDT+ Connector for Debug only

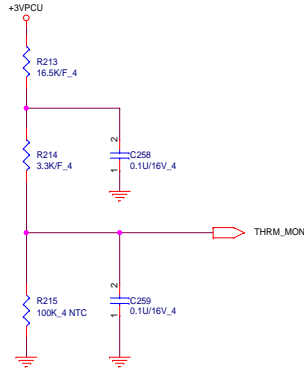
Can remove on MP



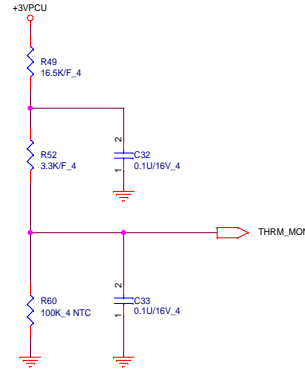
Close to HDT & No remove.

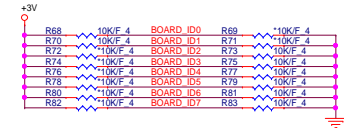
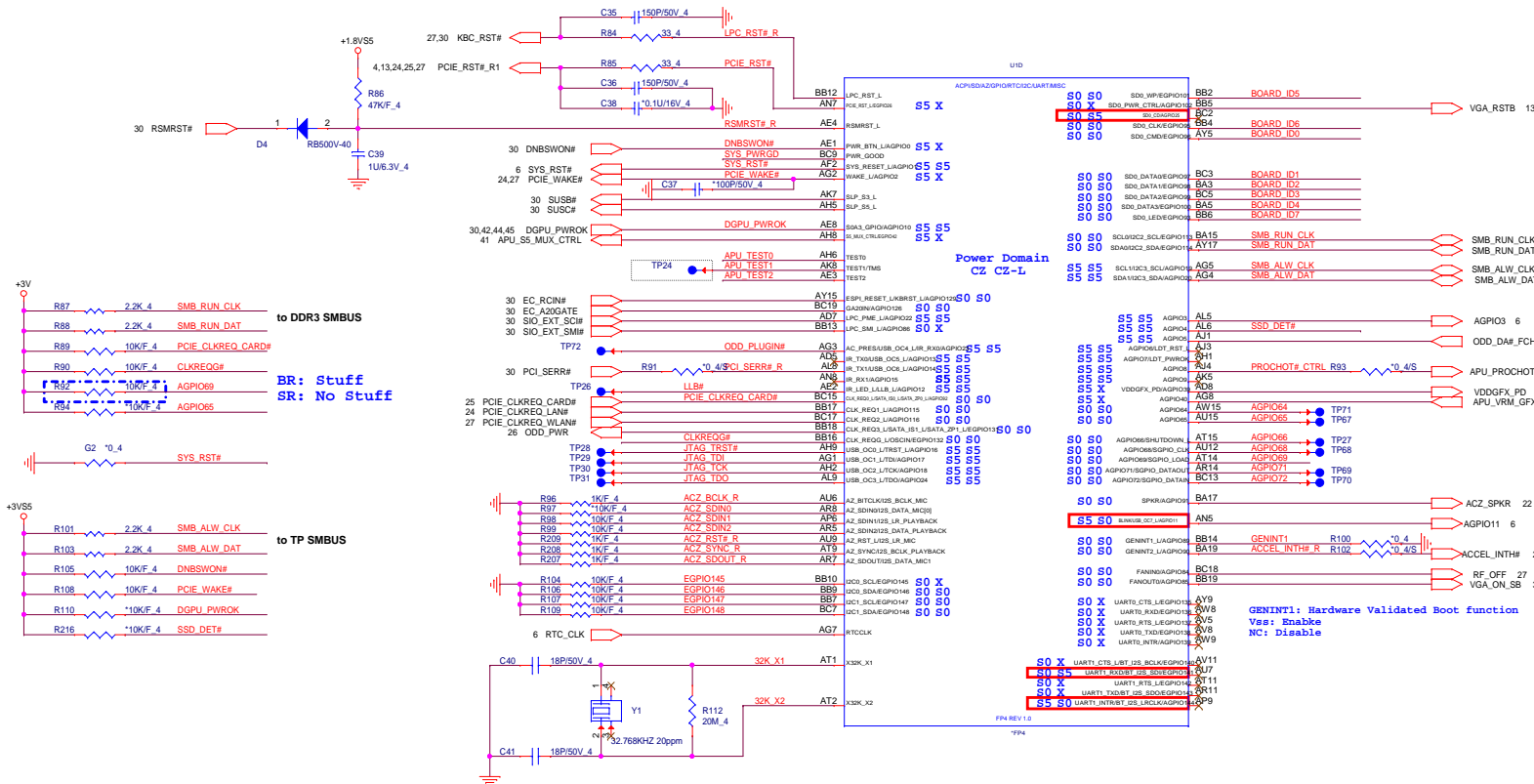


CPU Thermal Protect



Pipe Thermal Protect





BOARD ID SETTING

Board ID 0	Definition
0	UMA
1	DIS

Board ID [2:1]	Definition
00	14"
01	15"
10	17"
11	Reserve

Board ID [4:3]	Definition
00	Pavilion
01	Reserve
10	Reserve
11	Reserve

Board ID [5]	Definition
0/1	BR/SR

Board ID [6]	Definition
0/1	Reserve

Board ID [7]	Definition
0/1	Reserve

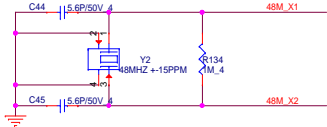
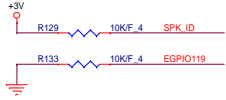
TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



PROJECT : G54A
Quanta Computer Inc.

Size Document Number
BR & SR 47(GPIO/AZ/UART) Rev 1A
Date: Monday, January 11, 2016 Sheet 5 of 46

Follow Checklist



30 CLK_33M_KBC
27 CLK_PCI_TPM
27 CLK_33M_DEBUG

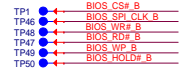
For EMI



APU SPI ROM

Vender	Size	P/N (1.8V)
WIND	8M	AKE5EZNON00
EON	8M	AKE5EFNOQ00
	8M	
Socket	DFHS08FS023	

TPs need place to all TOP or all BOT

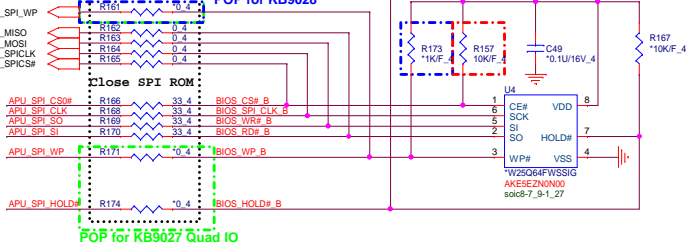


POP for KB9027 Quad IO

POP for KB9028

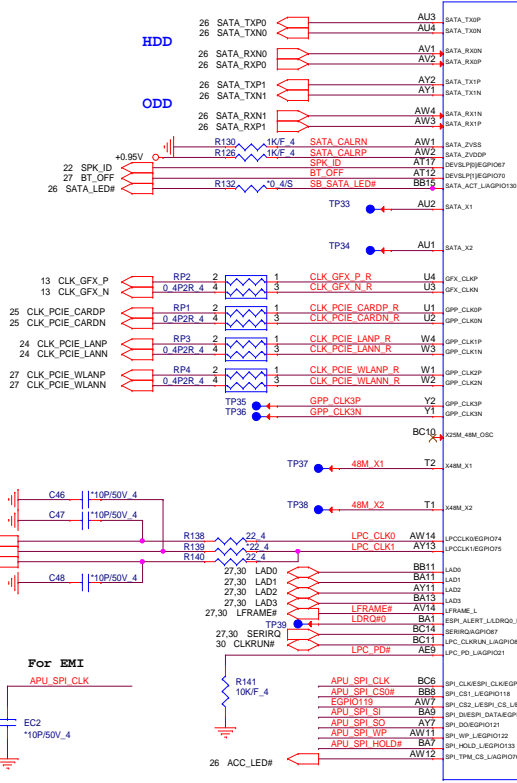
POP for KB9028

MUST STUFF



POP for KB9027 Quad IO

U1E

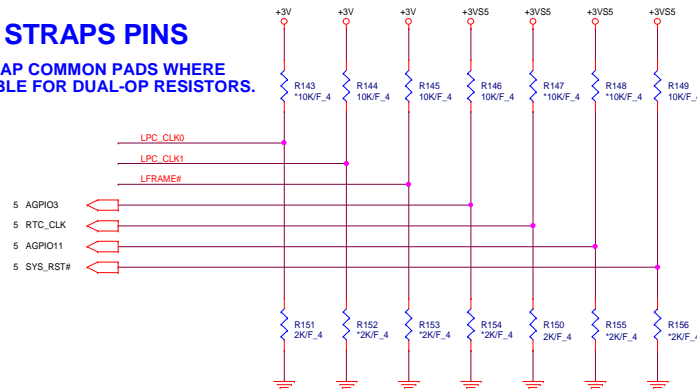


FPGA REV 1.0

*FPGA

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



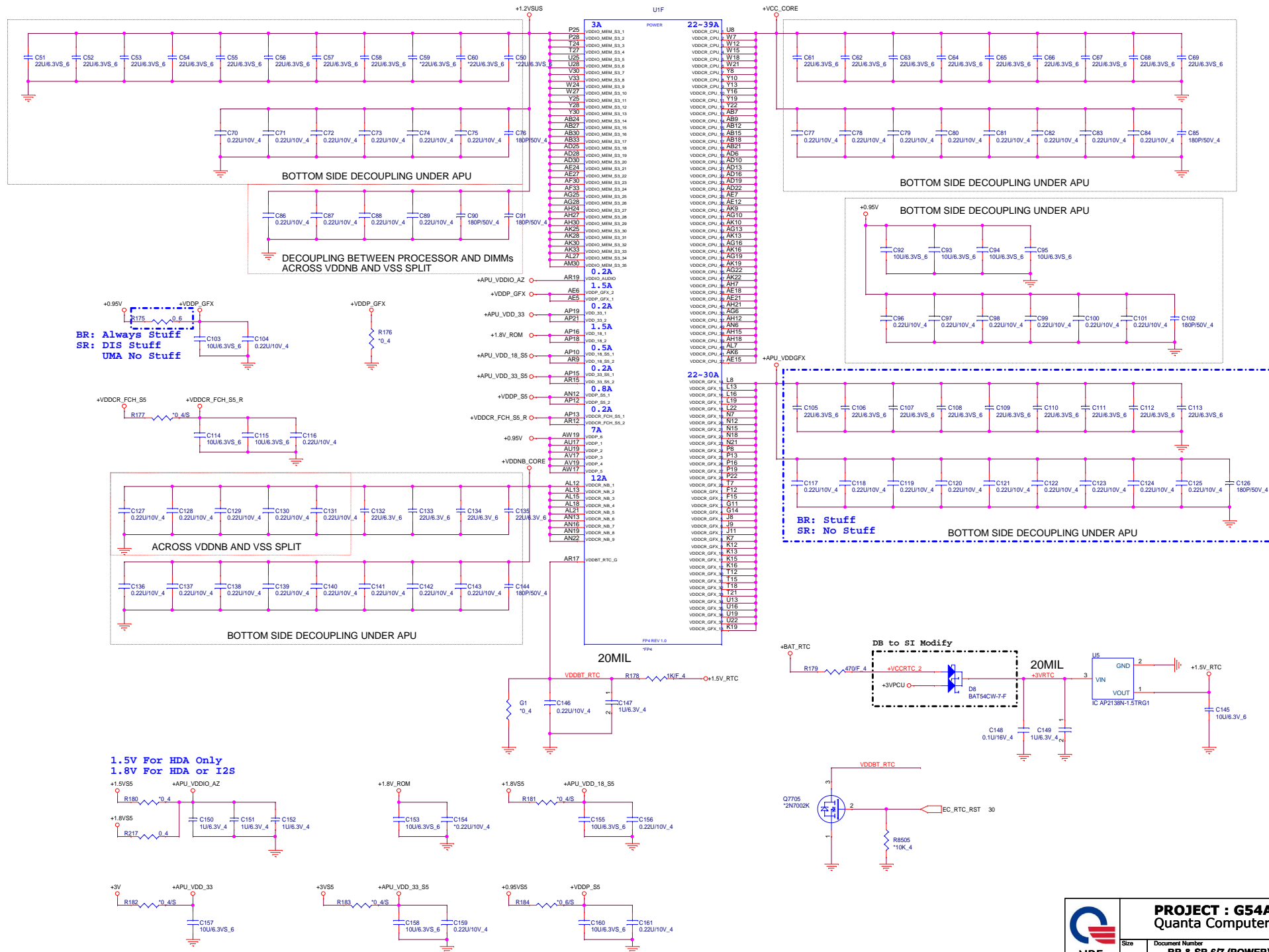
REQUIRED STRAPS

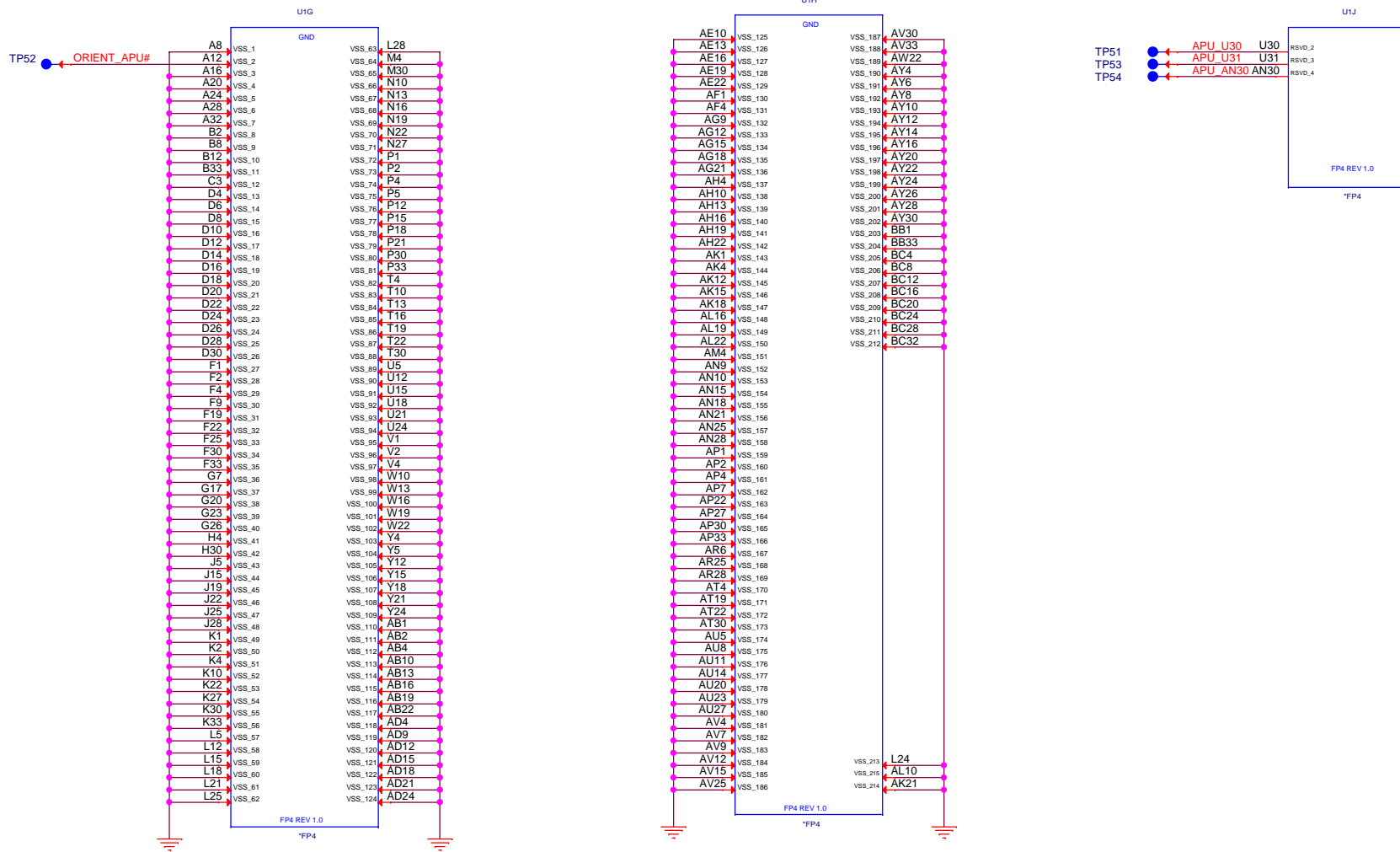
	LPC_CLK0	LPC_CLK1	LFRAME#	AGPIO3 <small>in Pull-Up</small>	RTC_CLK <small>in Pull-Up</small>	AGPIO11=BLINK <small>in Pull-Up</small>	SYS_RST# <small>in Pull-Up</small>
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks <small>DEFAULT</small>	SPI ROM <small>DEFAULT</small>	1.8V SPI ROM Enhanced reset logic (for quicker S5 resume) <small>DEFAULT</small>	Coin battery is on board. normal reset mode output to APU <small>DEFAULT</small>	LDT_RST#/LDT_PWRGD output to Pads <small>DEFAULT</small>	normal reset mode <small>DEFAULT</small>
PULL LOW	BOOT FAIL TIMER DISABLED <small>DEFAULT</small>	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC ROM	3.3V SPI ROM Default to traditional reset logic <small>DEFAULT</small>	Coin battery is not on board.	LDT_RST#/LDT_PWRGD output to Pads <small>DEFAULT</small>	short reset mode output to Pads <small>DEFAULT</small>



PROJECT : G54A
Quanta Computer Inc.

Size	Document Number	Rev
NB5	BR & SR 5/7(SATA/USB/SPI)	1A
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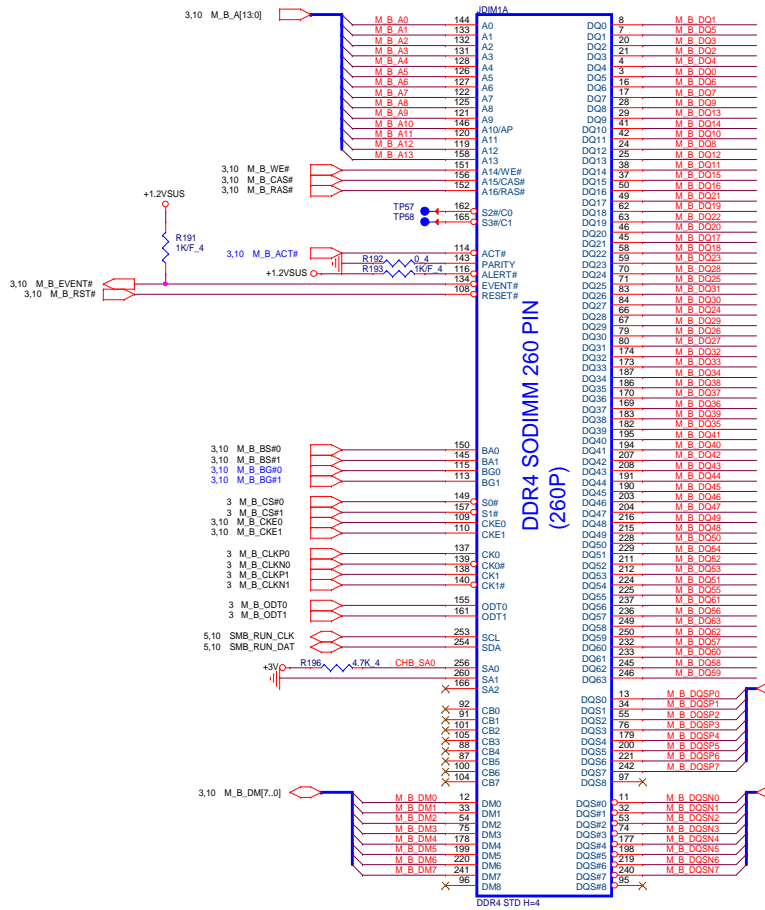


PROJECT : G54A
Quanta Computer Inc.

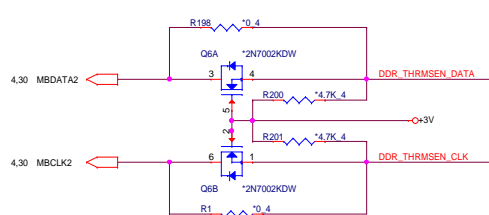
Size	Document Number	Rev
	BR & SR 7/7 (GND)	1A
Date: Monday, January 11, 2016	Sheet 8 of 46	

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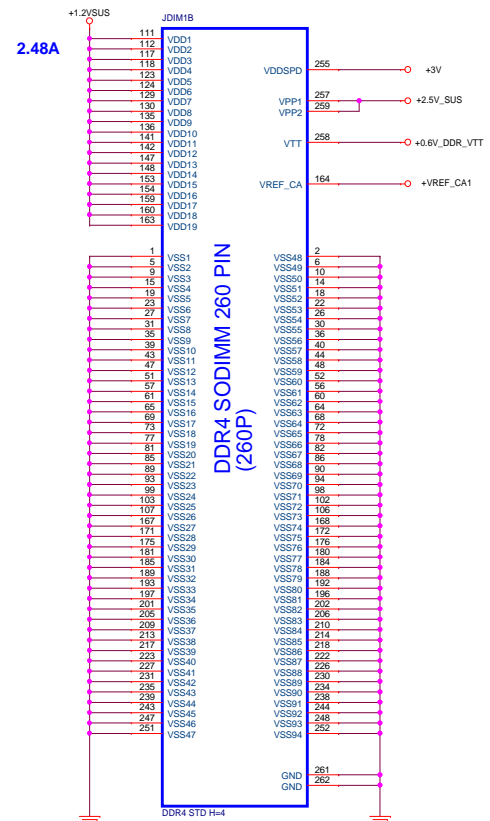
	PROJECT : G54A Quanta Computer Inc.		
	Size A	Document Number Reserved	Rev 1A
	Date: Monday, January 11, 2016		Sheet 9 of 46



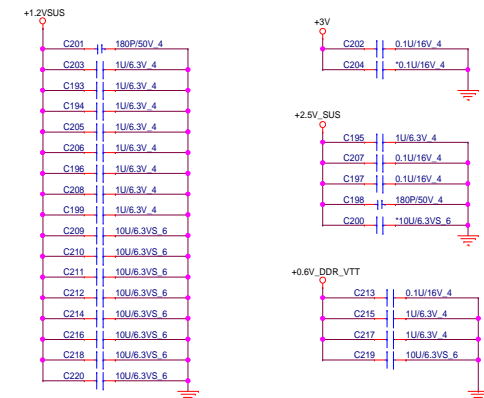
Local Thermal Sensor



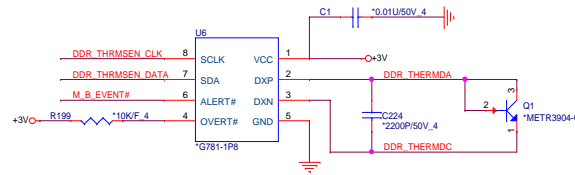
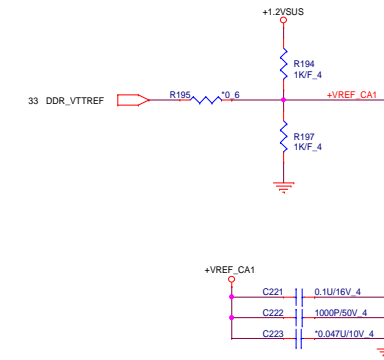
M_B_DQ[63:0] 3.10



Place these Caps near SODIMM



1uF/10uF 4pcs on each side of SODIMM




Main:AL000781039 G781-1P8(9Ah)
 2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)
 Main:AL001412003 EMC1412-1-ACZL-TR(98h)
 2nd:AL000431014 TMP431ADGKR(98h)

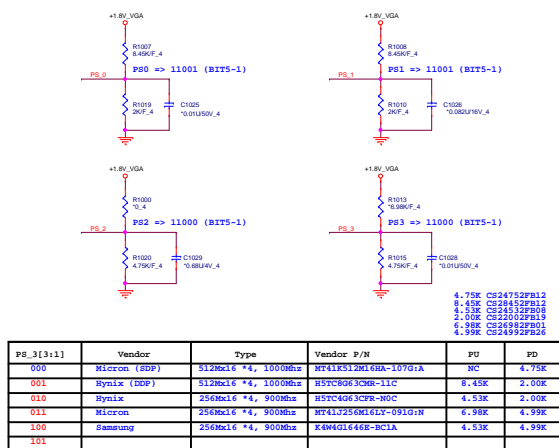
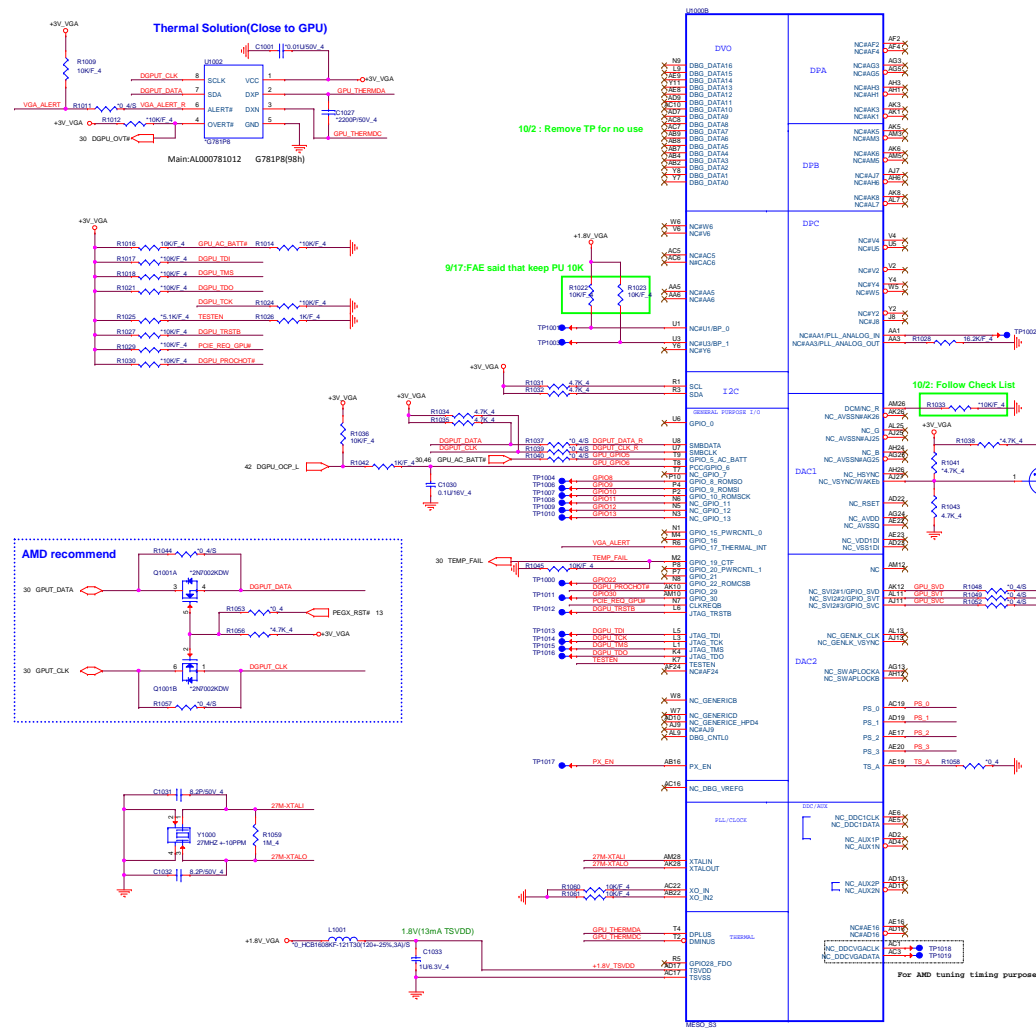


PROJECT : T15-BA
Quanta Computer Inc.

Size C Document Number
CHB DDR4 DIMM1-STD(4.0H)
 Date: Monday, January 11, 2016 Sheet 11 of 46

<Reserved for CHB - DIMM2>

 NB5	PROJECT : G54A Quanta Computer Inc.		
	Size A	Document Number CHB DDR4 DIMM2-RVS(4.0H)	Rev 1A
	Date: Monday, January 11, 2016		Sheet 12 of 46



PS PS Implementation

- Connect GPD_2B to 10K pull-down to enable HUPS
- Value of PS_0 (102) is not used, leave "No connect"
- R, pu, R, pd and C must be properly populated per tables below
- Place HUPS circuit component as close to the PS pin as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistor should be of +/-5% tolerance

Capacitor Lookup Table

C (pF)	ESR (Ohm)	R,pu (Ohm)	R,pd (Ohm)	ESR (Ohm)
000	80	NC	4750	000
01	10	8450	2000	000
10	10	4030	2000	000
NC	11	0980	8990	001
		4730	4990	100
		1340	500	100
		3400	10000	110
		4750	NC	111

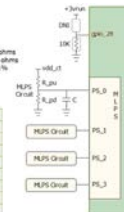
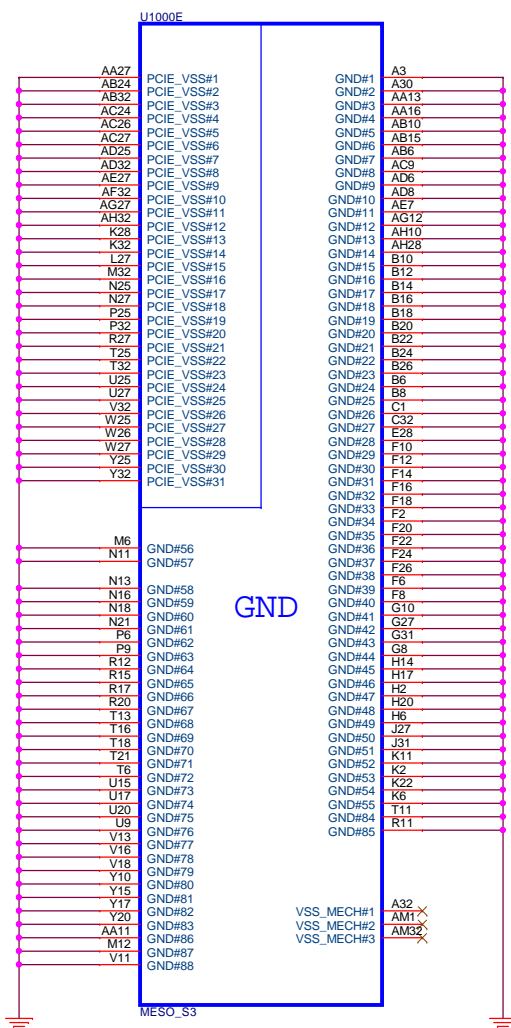


Table 3-24 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures ROM_CONFIG[2:0]

Size	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

NLPS Bit	Strap Name	Description	Recommended Settings
PS_H01	ROM_CONFIG[0]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[0] defines the ROM type.	Design dependent, use the description.
PS_H02	ROM_CONFIG[1]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[1] defines the primary memory aperture size. See Table 3-24 Primary Memory Aperture Sizes.	Design dependent, use the description.
PS_H03	ROM_CONFIG[2]	Reserved for internal use only. Must be 1 at reset.	1
PS_H04	N/A	Reserved.	1
PS_H10	STRAP_BIF_GEN0_EN_A	1 = PCIe GEN3 capabilities. 0 = PCIe GEN3 is not supported.	Design dependent, use the description.
PS_H20	STRAP_BIF_CLK_PN_EN	1 = The CLKREQ# power management capability is enabled. 0 = The CLKREQ# power management capability is disabled.	0
PS_H30	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_H40	STRAP_TX_CFG_DRV_FULL_SWING	1 = The transmitter full-swing is enabled. 0 = The transmitter full-swing is disabled.	1
PS_H50	STRAP_TX_DEEMPH_EN	1 = Tx deemphasis enabled. 0 = Tx deemphasis disabled.	Design dependent, use the description.
PS_H101	N/A	Reserved.	0
PS_H201	N/A	Reserved.	0
PS_H202	N/A	Reserved.	0
PS_H203	STRAP_BIOS_ROM_EN	1 = Enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device.	Design dependent, use the description.
PS_H204	N/A	Reserved.	0
PS_H205	N/A	Reserved.	0
PS_H301	BOARD_CONFIG[0]	Board configuration related settings, such as for security ID.	Design dependent, use the description.
PS_H302	BOARD_CONFIG[1]	Reserved.	0
PS_H303	N/A	Reserved.	0



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

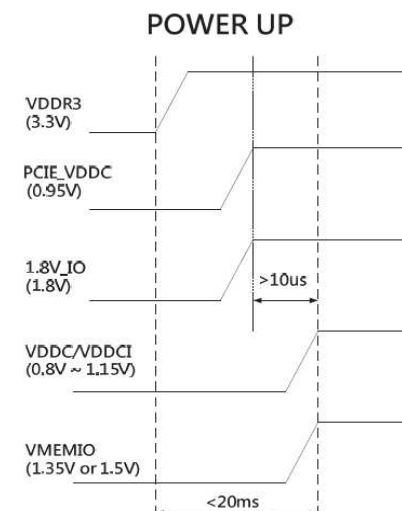
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

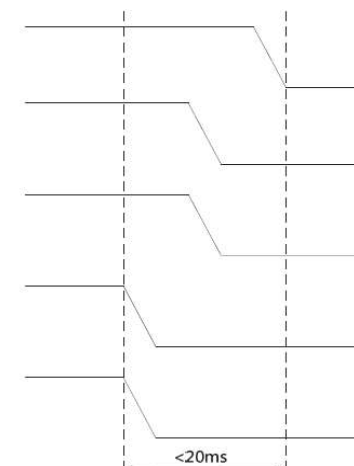
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE

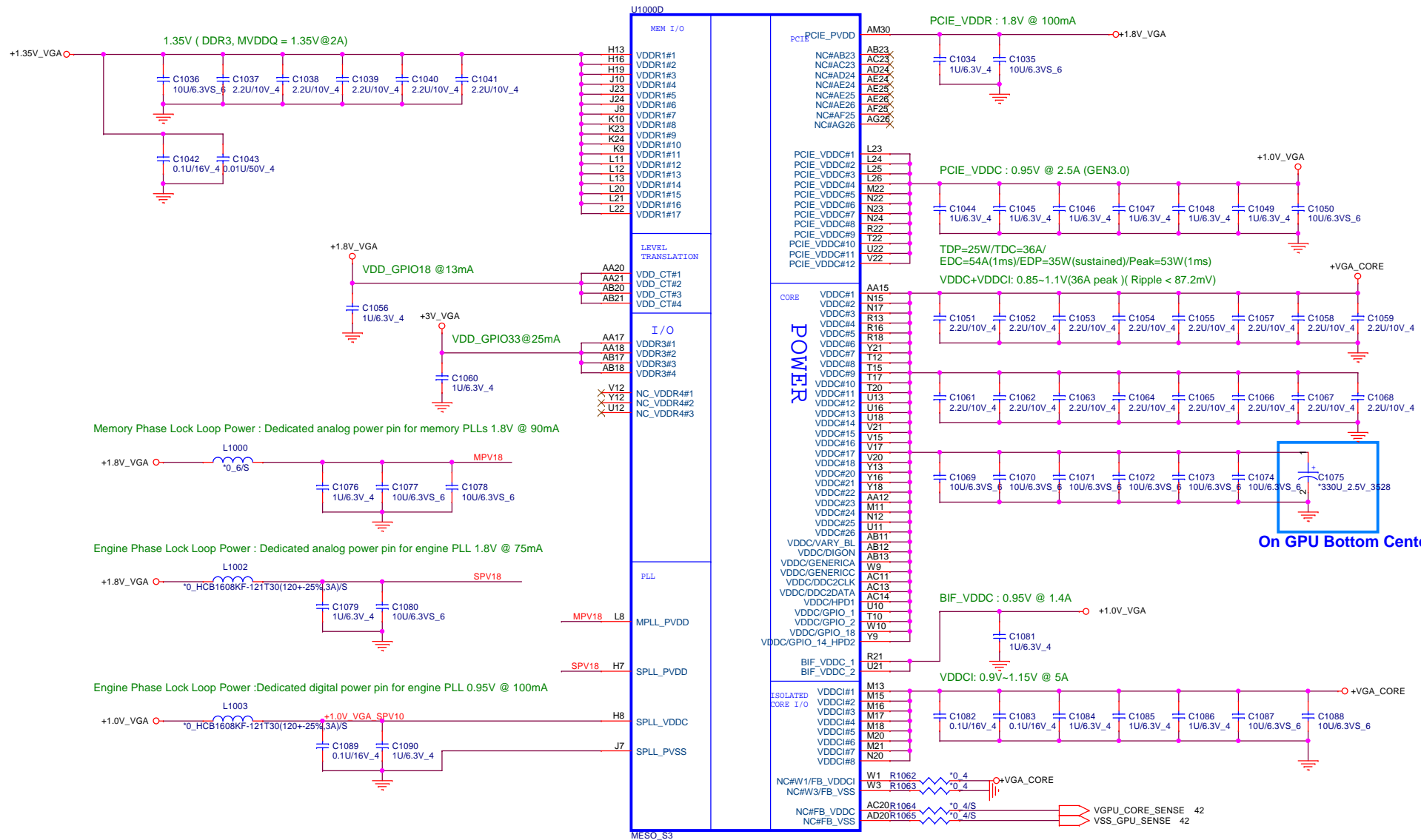


POWER DOWN



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Quanta Computer Inc.


Size	Document Number	Rev
	M1-70_S3_GND/LVDS/Strap	1A
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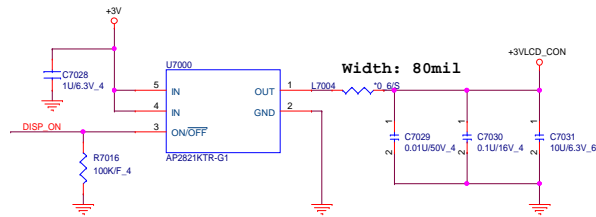
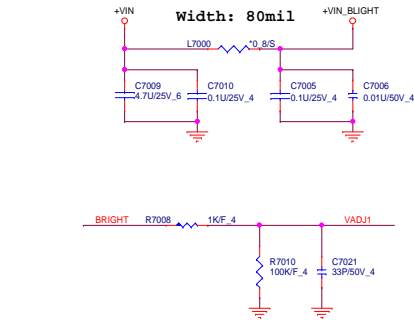
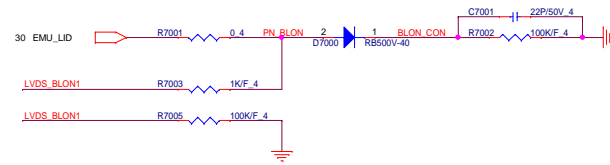
PROJECT : G54A
Quanta Computer Inc.

Size	Document Number	Rev
M1-70_S3_POWER		1A
Date: Monday, January 11, 2016	Sheet 16 of 46	

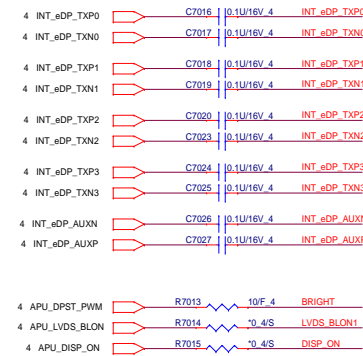
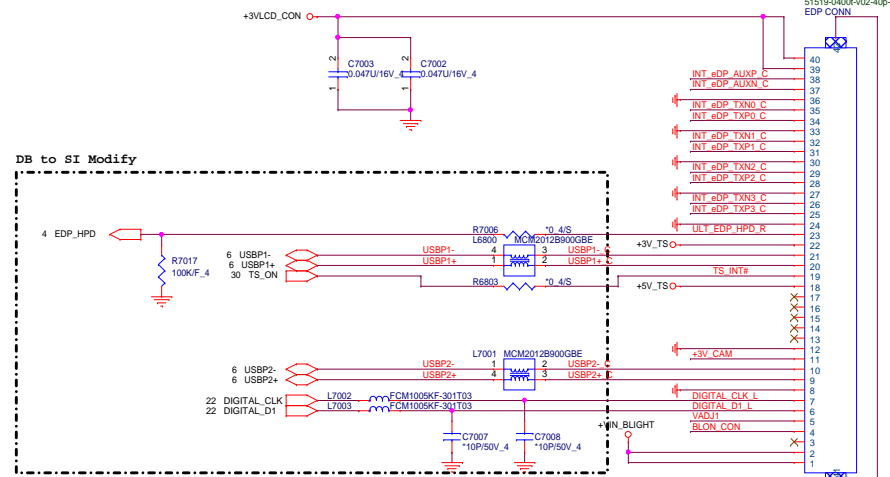
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 NB5	PROJECT : G54A Quanta Computer Inc.		
	Size A	Document Number Reserved	Rev 1A
	Date: Monday, January 11, 2016		Sheet 19 of 46

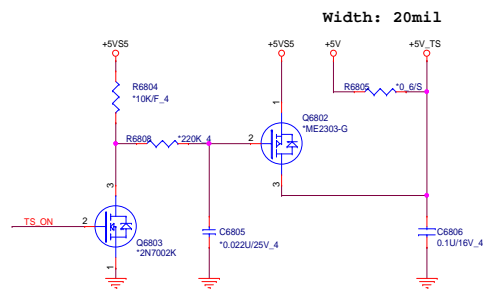
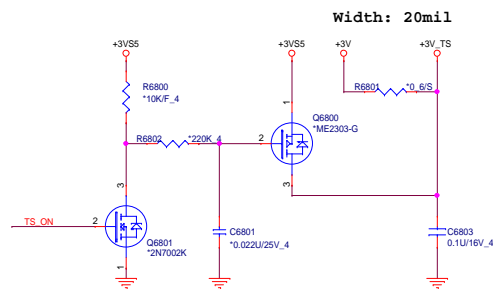
LID Switch



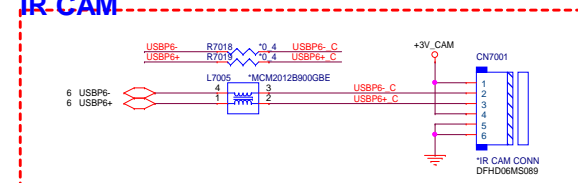
eDP CONN.

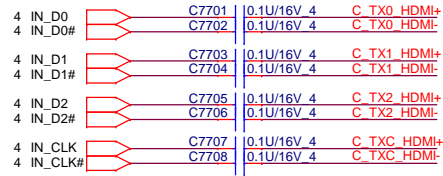


Touch screen

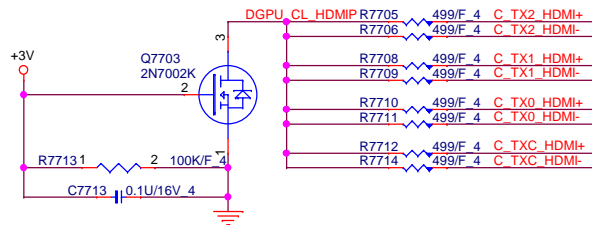
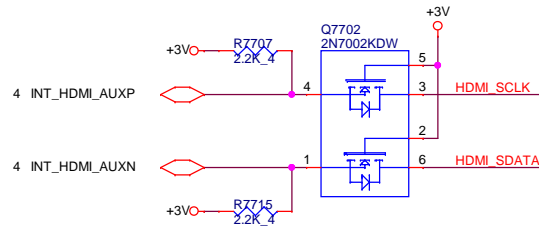


IR CAM





HDMI SMBus Isolation

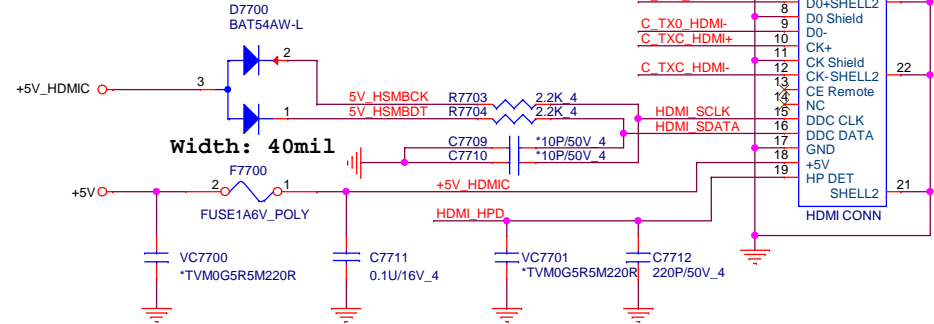


4 HDMI_HPQ_Q

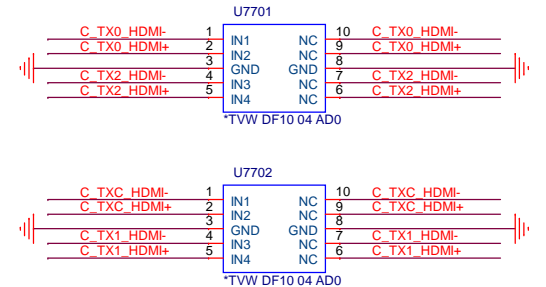
2KV ESD protection

DB to SI Modify

For EMI

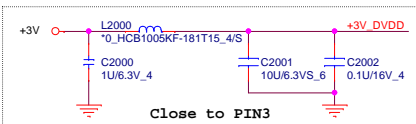


DB to SI Modify

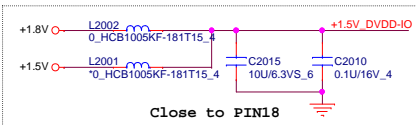


PROJECT : G54A
Quanta Computer Inc.

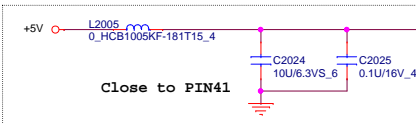
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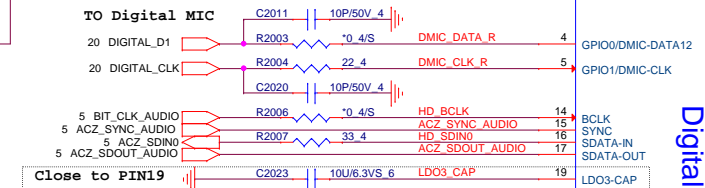
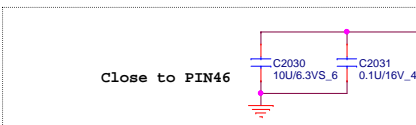
30mA



10mA

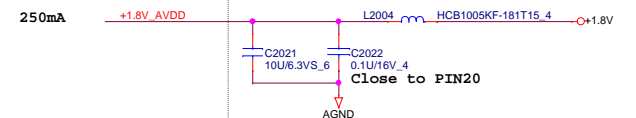
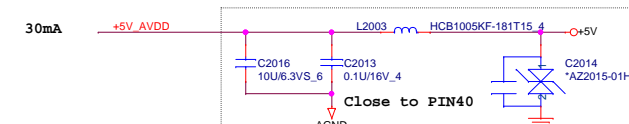
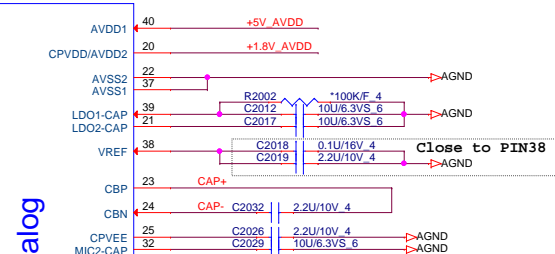


1000mA



Digital

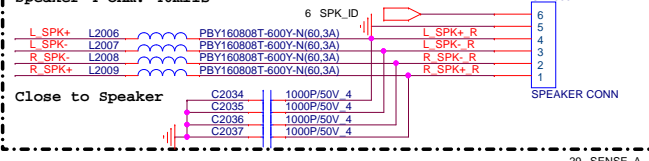
Analog



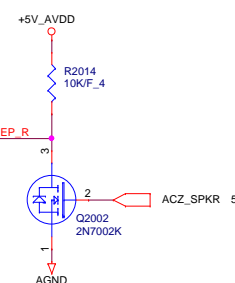
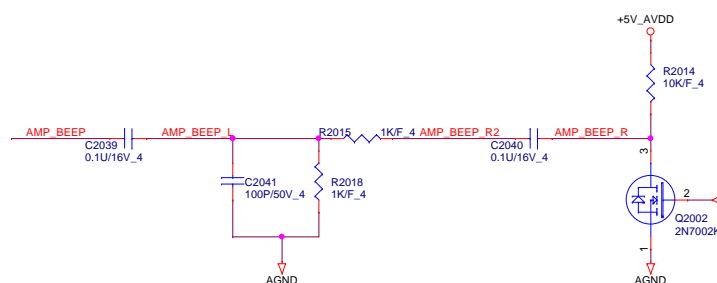
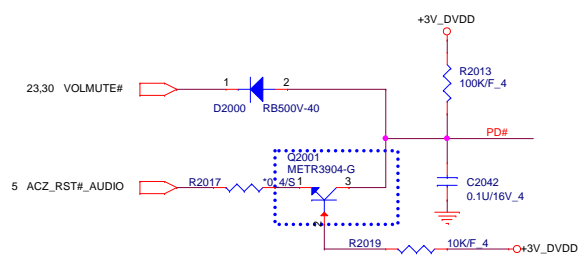
250mA

DB to SI Modify

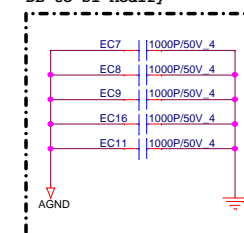
Speaker 4 ohm: 40mils



Speaker 4 ohm: 40mils



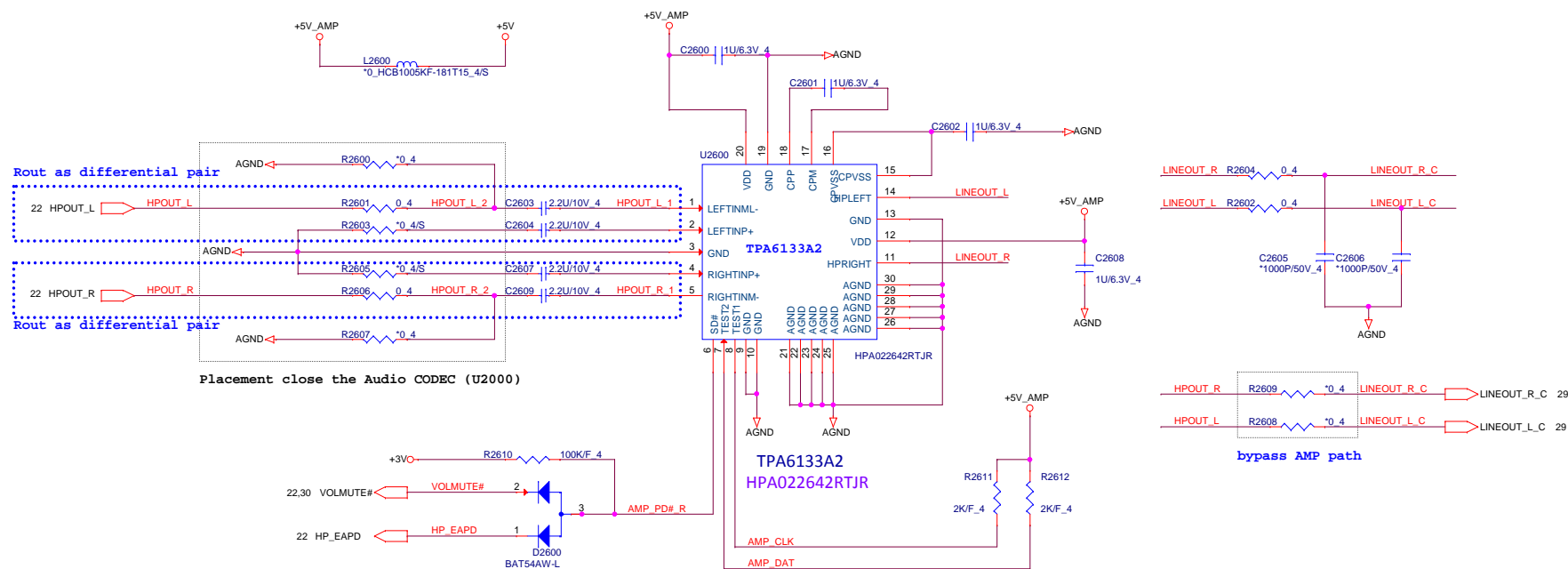
DB to SI Modify

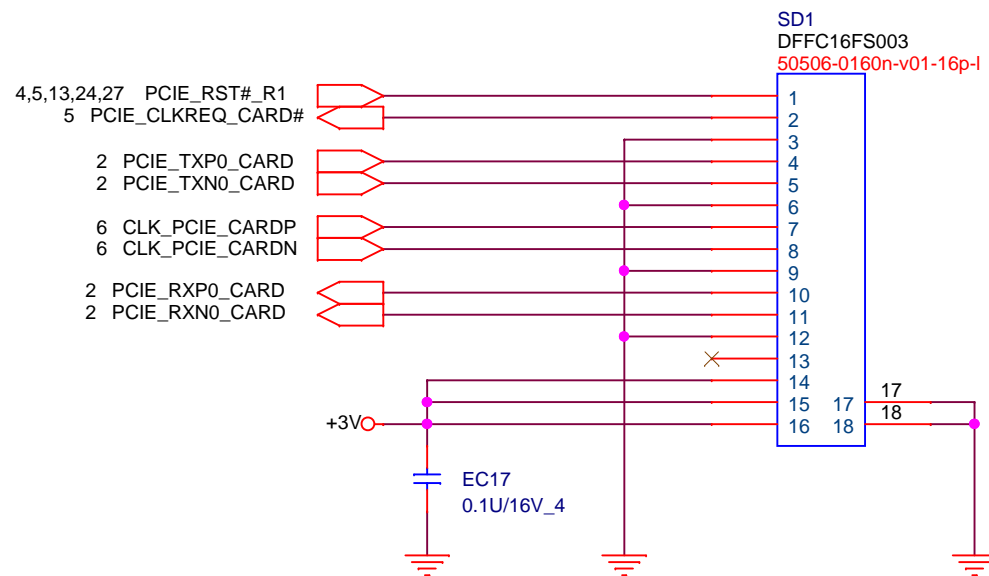


place to near or under codec

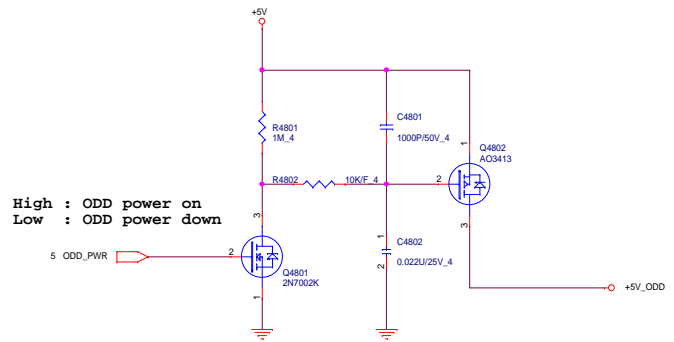
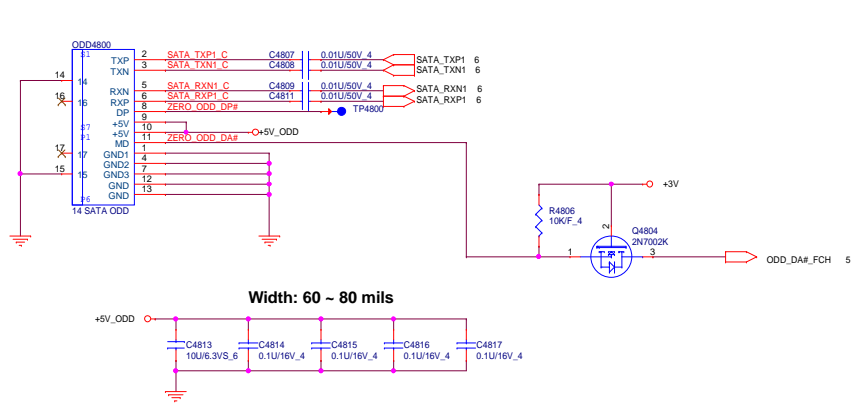


Head Phone Out

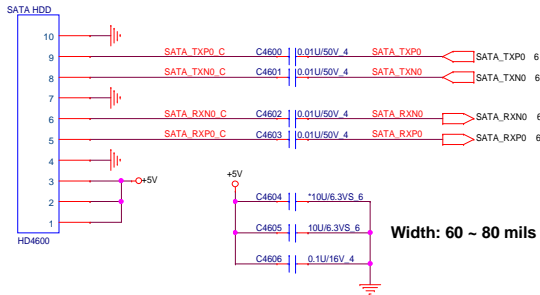




SATA ODD

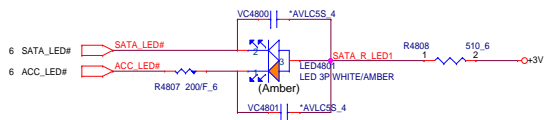


SATA HDD

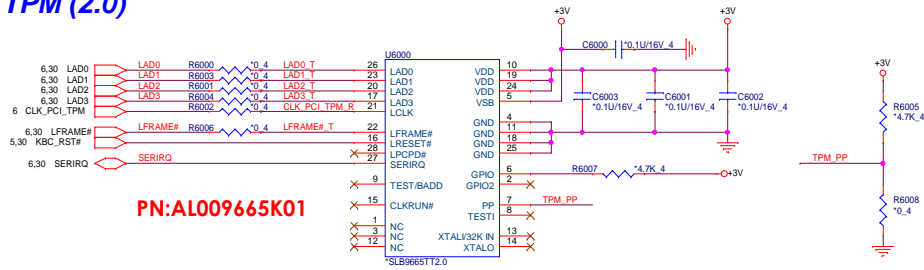


SATA SSD

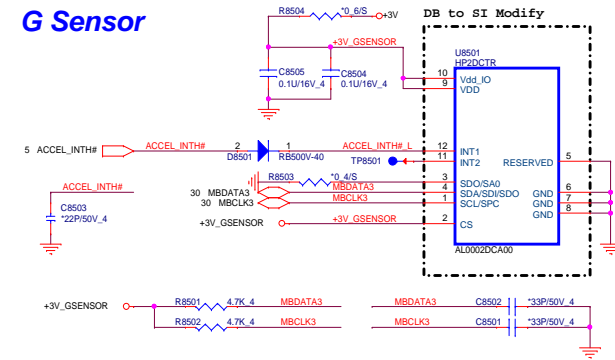
SATA LED



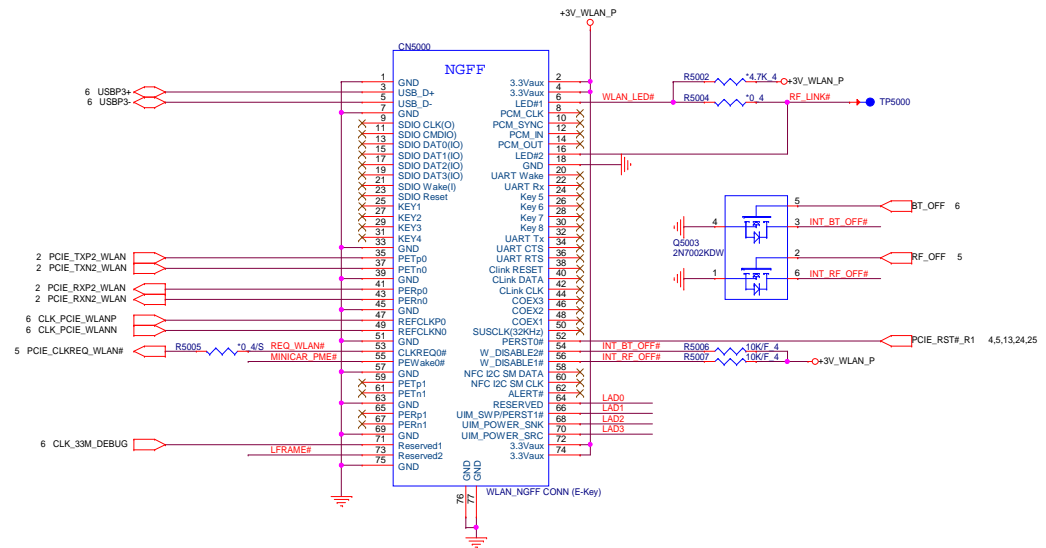
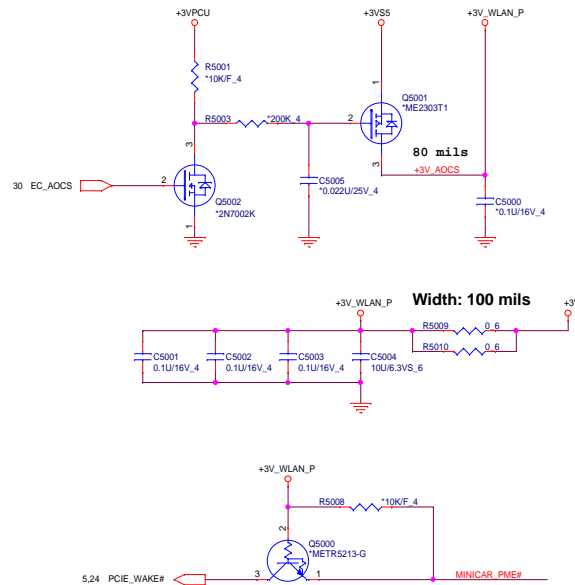
TPM (2.0)



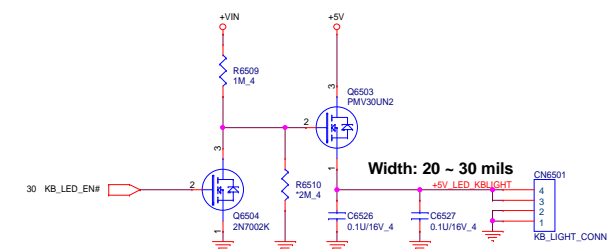
G Sensor



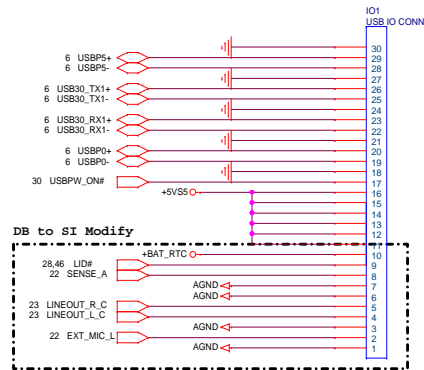
WLAN & BT



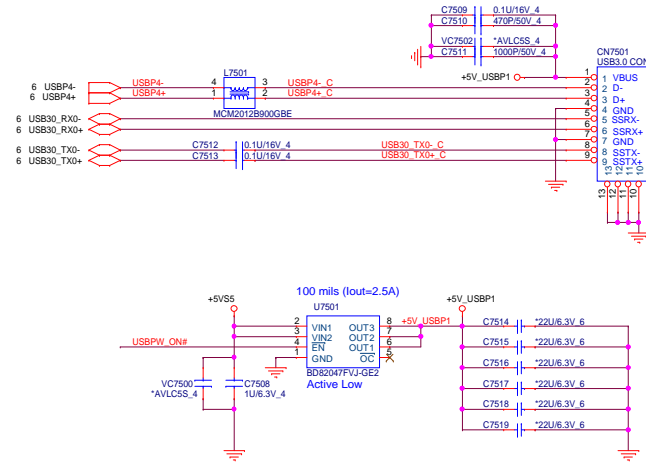
FAN CONN.



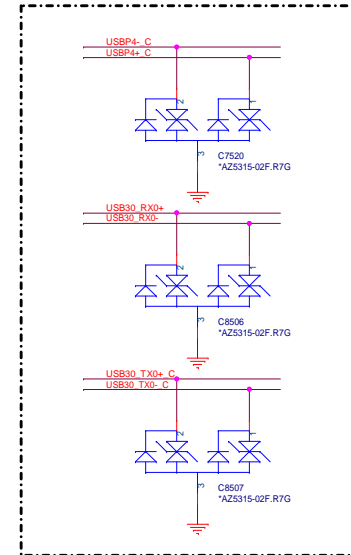
IO CONN.



USB3.0 CONN.

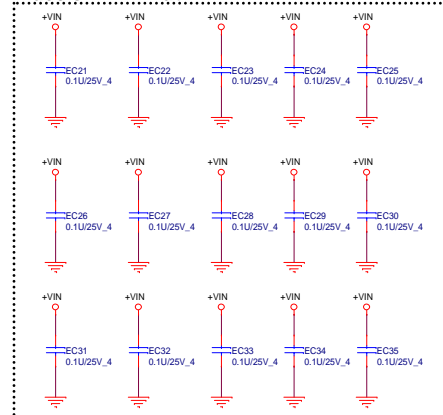


DB to SI Modify



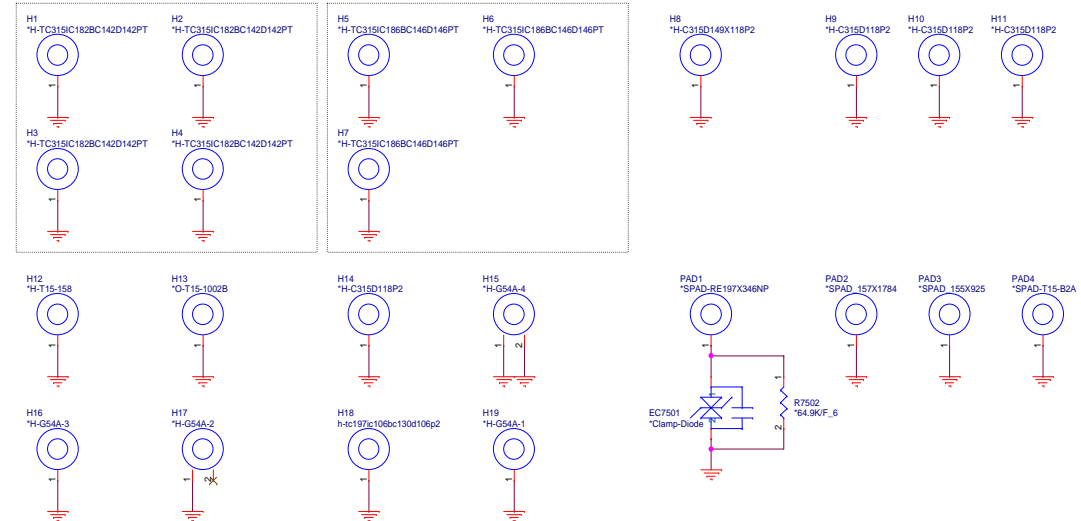
EMI CAPs

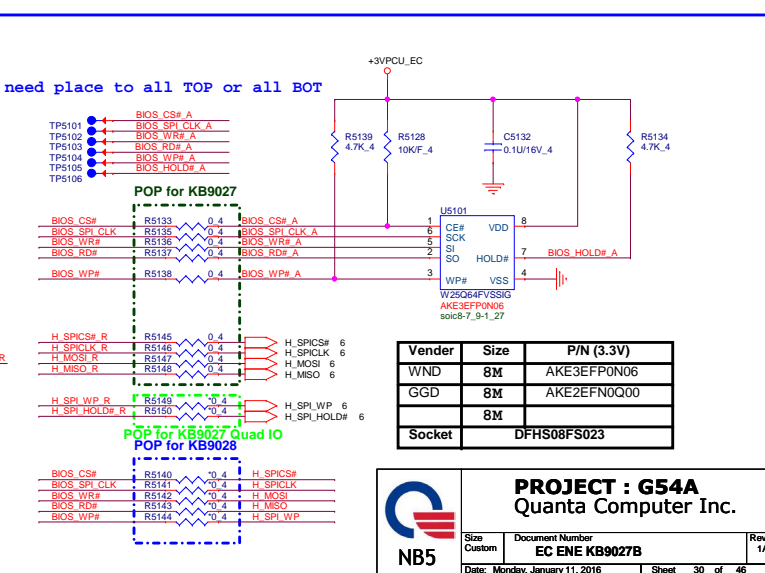
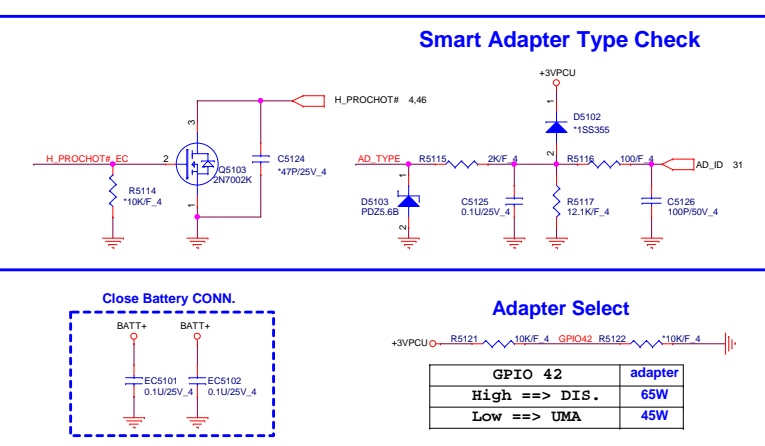
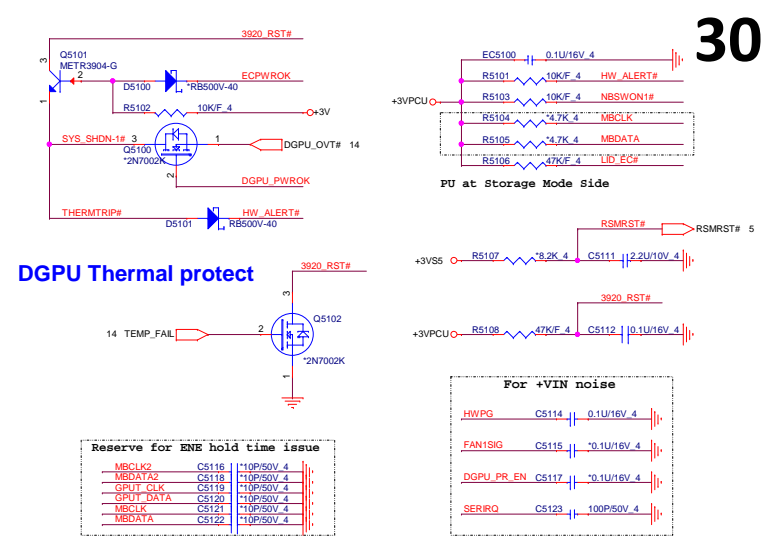
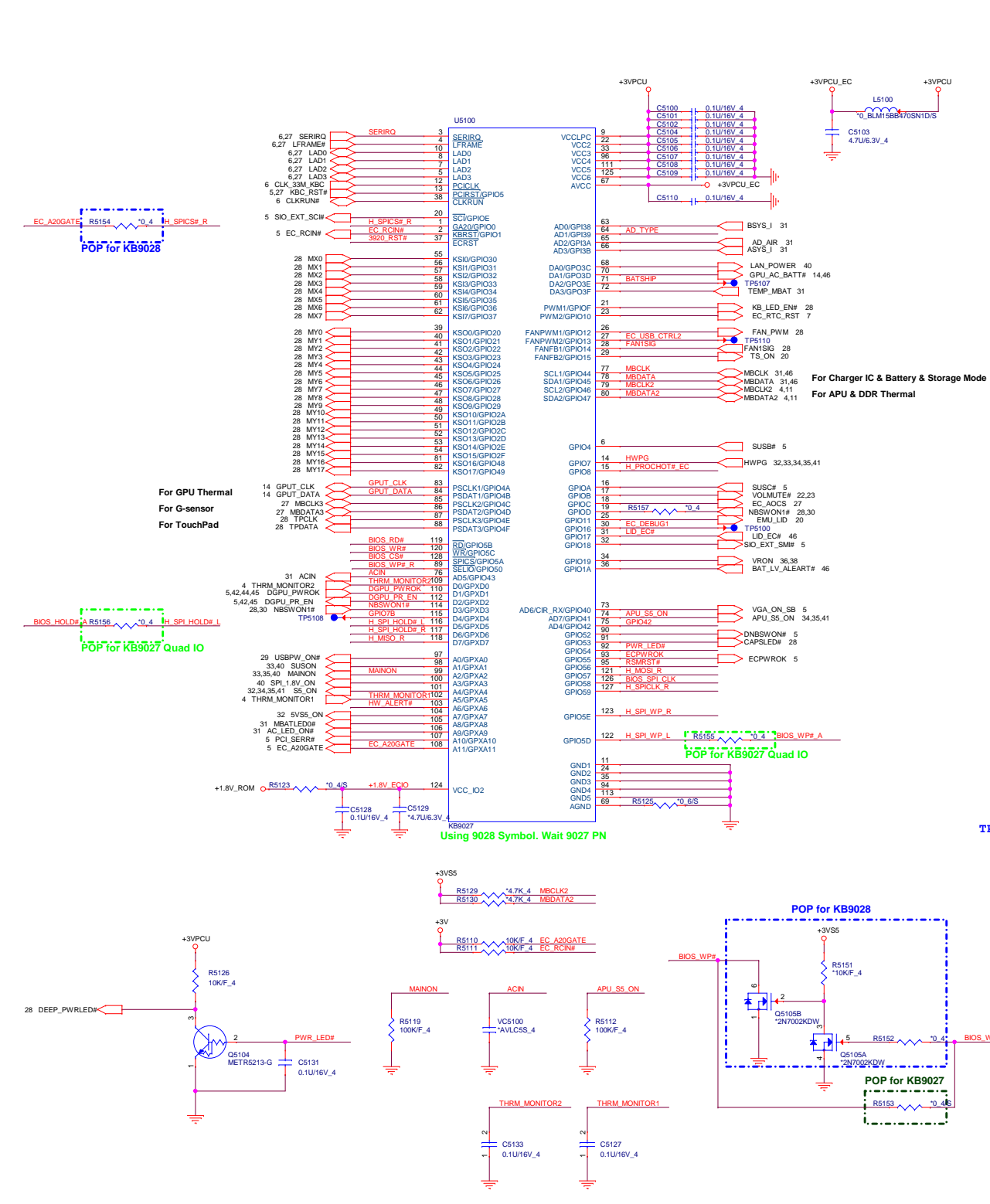
Place on +VIN Path



For ISN

HOLES & PADs





Vender	Size	P/N (3.3V)
WND	8M	AKE3EFP0N06
GGD	8M	AKE2EFN0Q00
	8M	
Socket	DFHS08FS023	

DC_JACK
90W

Place this ZVS close to
Diode away +VIN

Do Not add test pad on BATDIS_G signal

+BAT_RTC

31

2S1P 41Wh

Place this cap
close to EC

6V 15A

Place this cap
close to EC

Place this cap
close to EC

Place this cap
close to EC

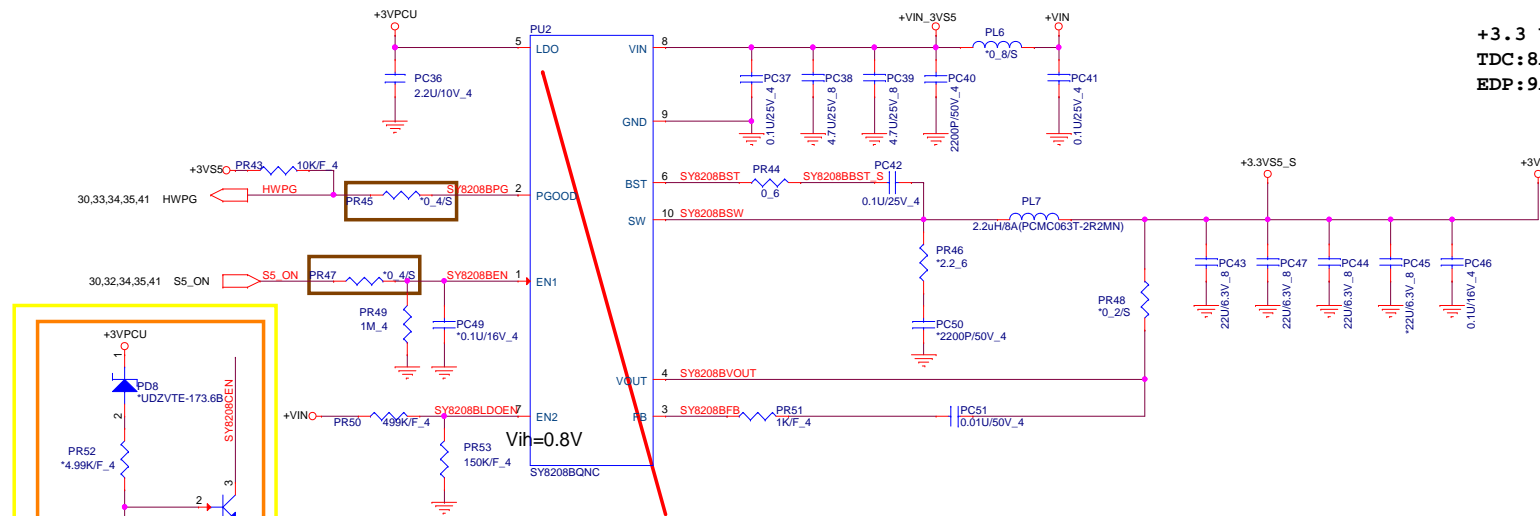
F_{sw}=614Khz

default setting 2S battery and NVDC

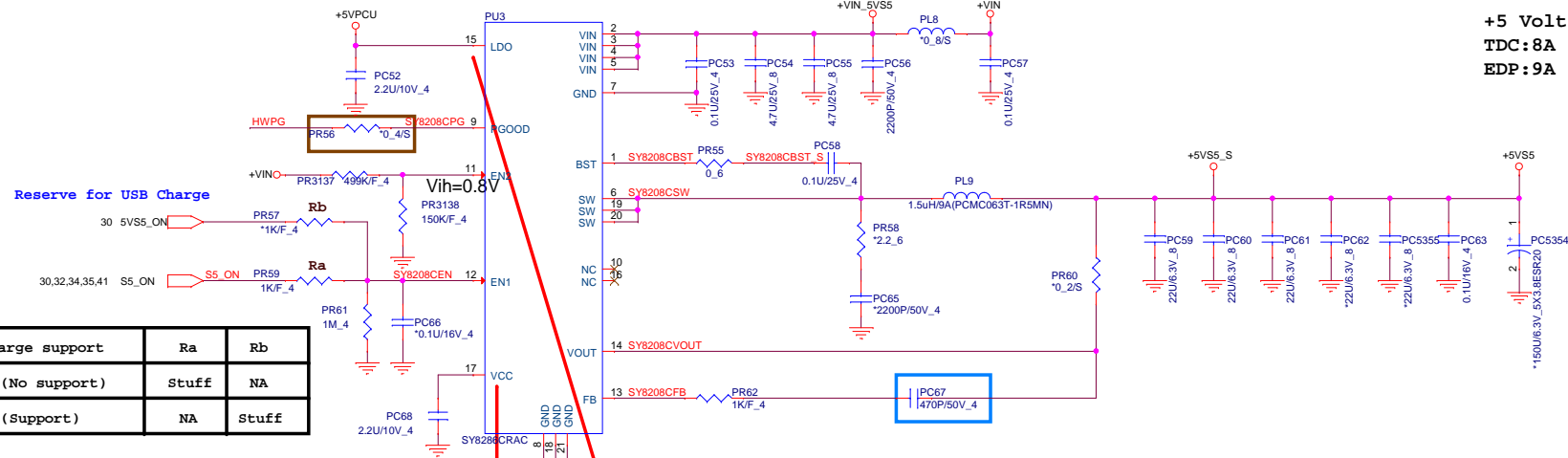
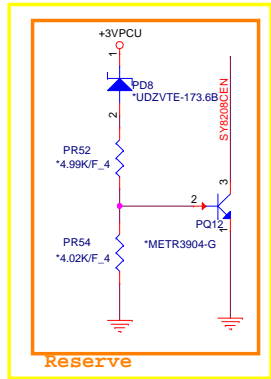


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Quanta Computer Inc.

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Custom	Charger (ISL88750)	1A
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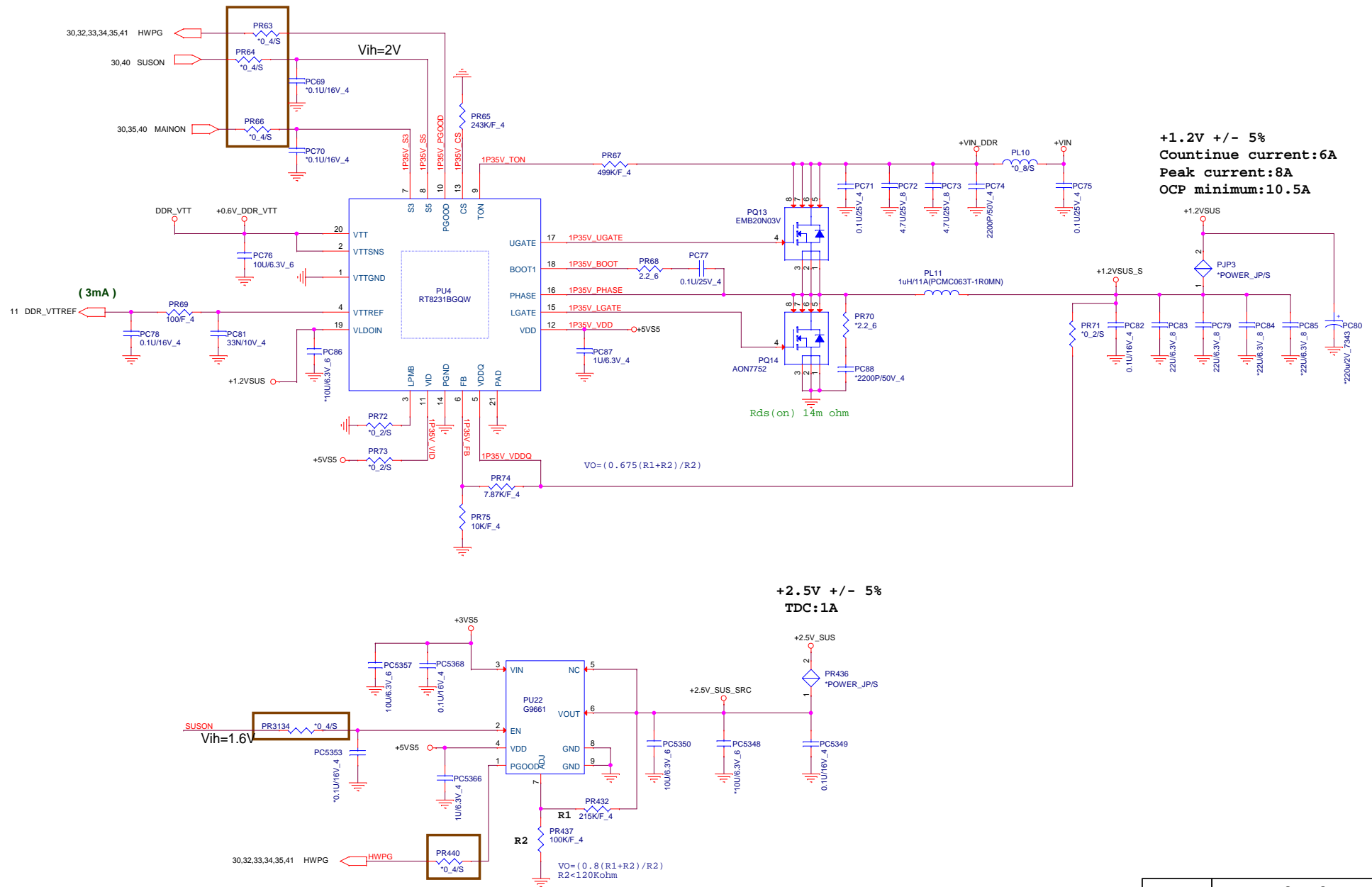


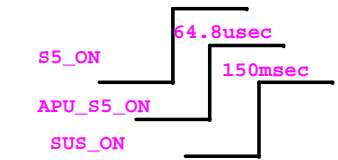
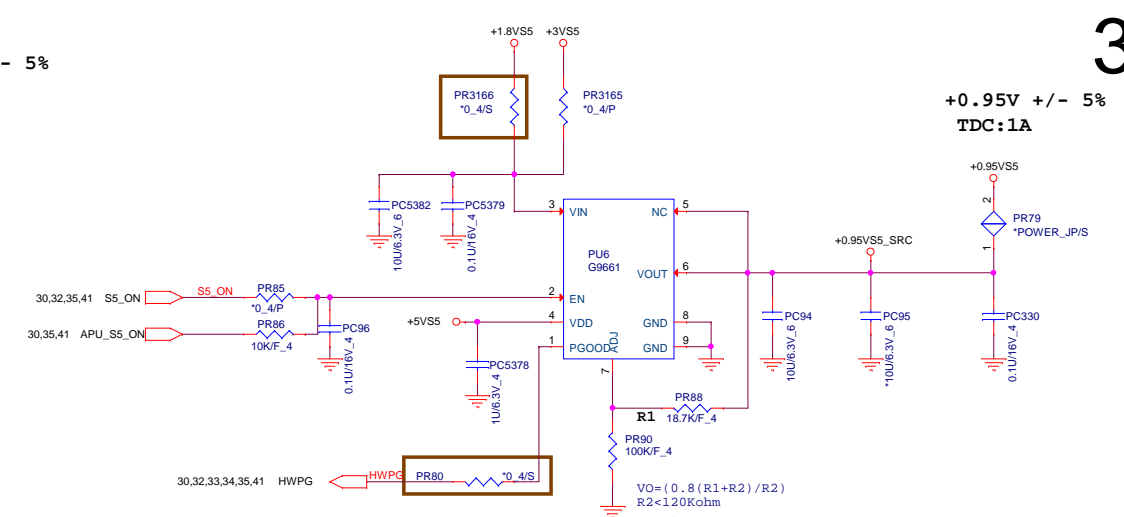
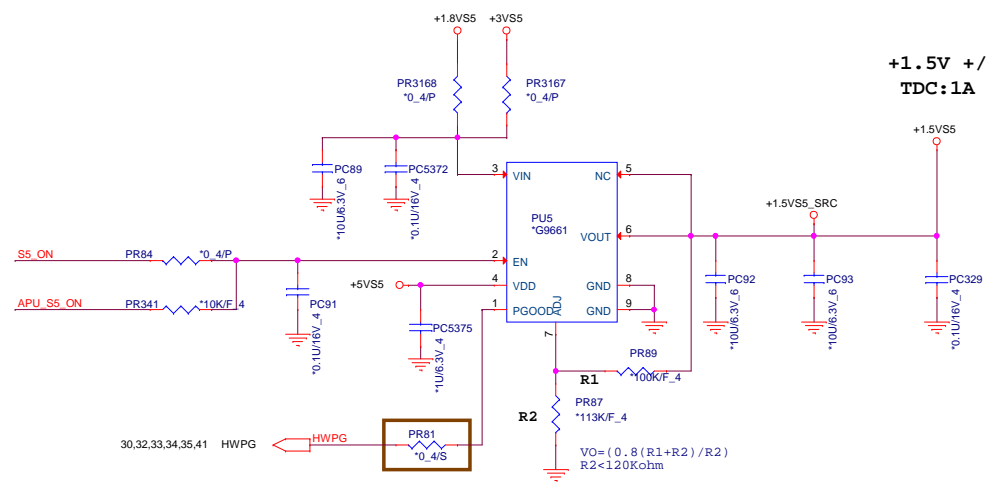
Do Not add test pad on VCC & LDO pin



Do Not add test pad on VCC & LDO pin

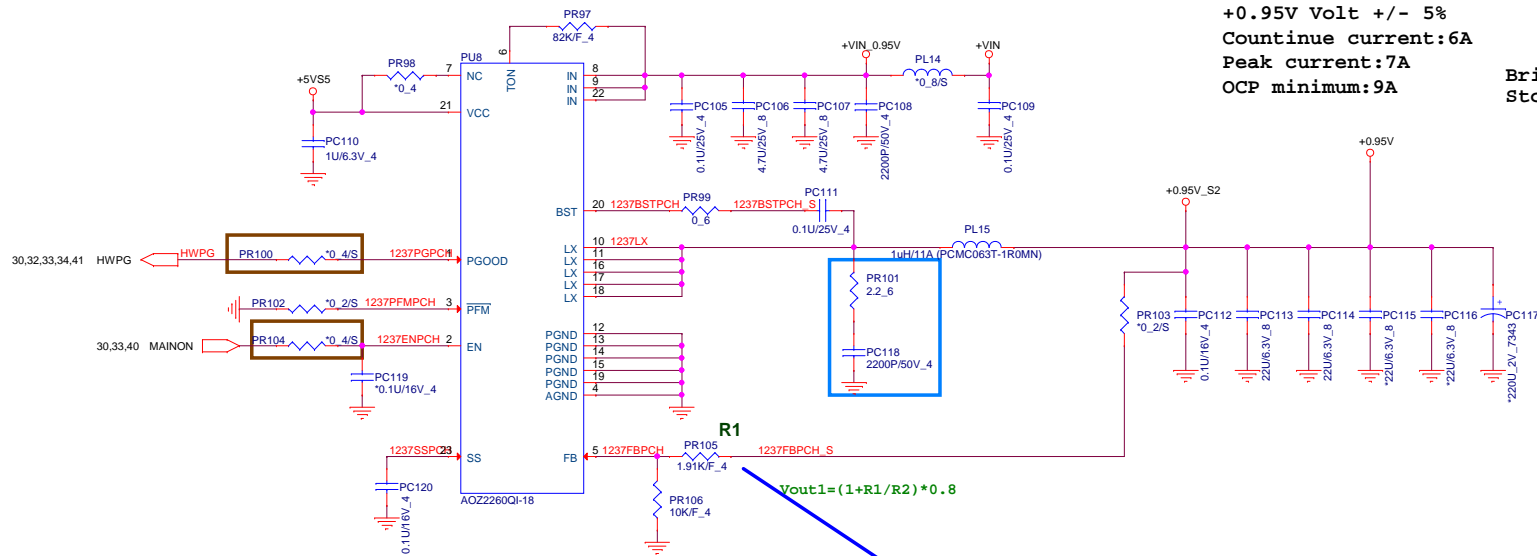
USB Charge support	Ra	Rb
Vine (No support)	Stuff	NA
Envy (Support)	NA	Stuff





	R1		
Stoney	18.7K	CS31872FB19	0.95V
Bristol	31.6K	CS33162FB14	1.05V

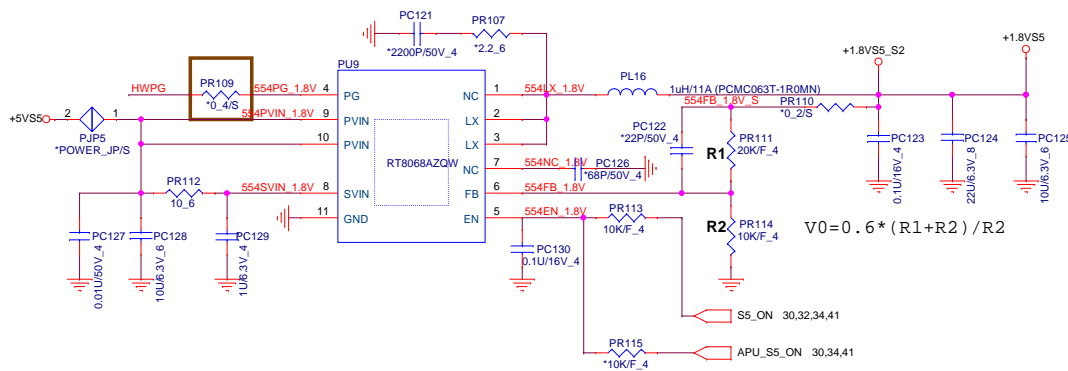
Bristol VDDP=1.05V
Stoney VDDP=0.95V

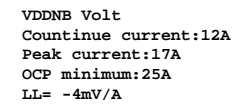
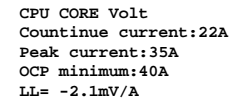


Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

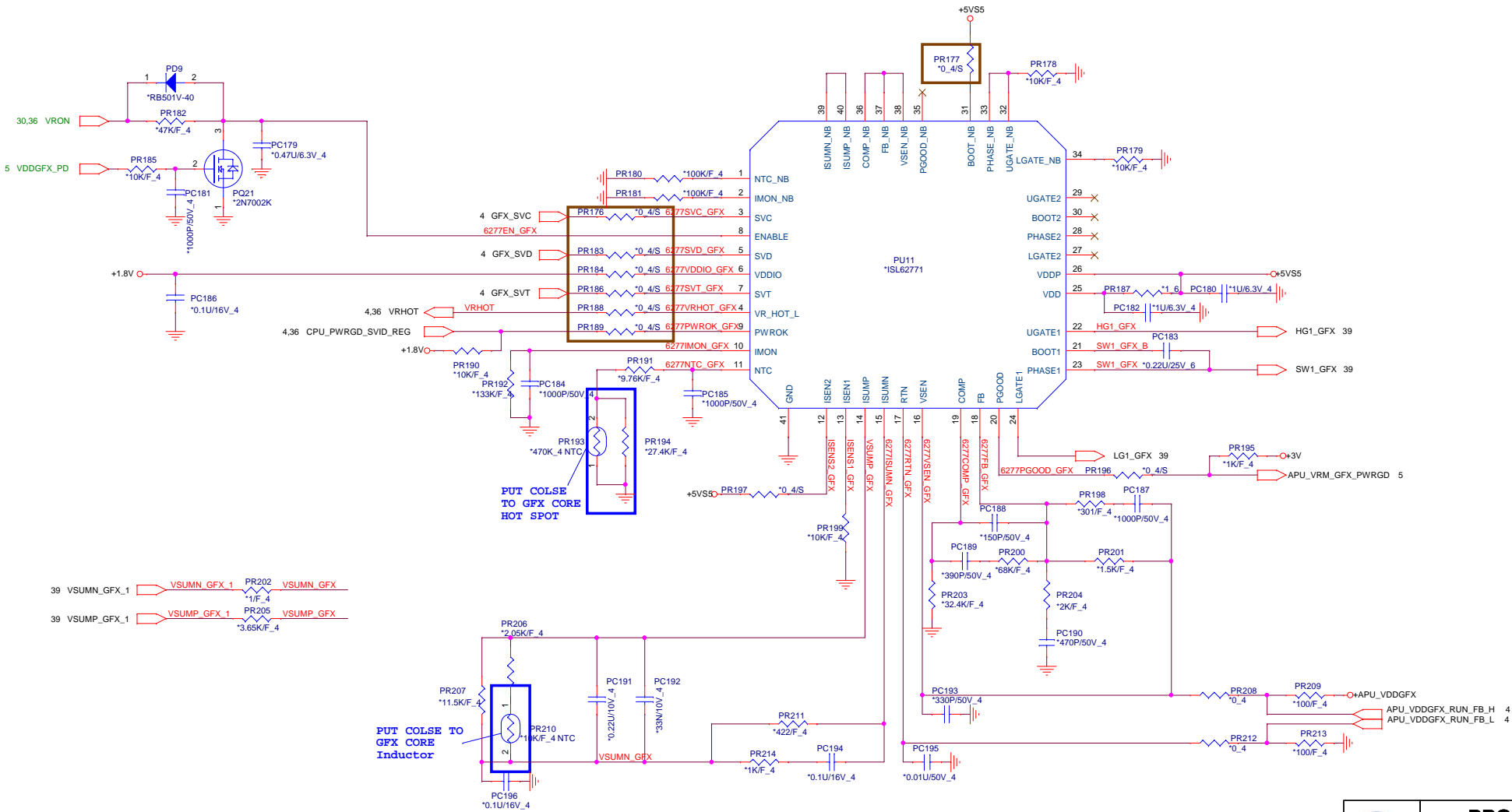
	R1		
Stoney	1.91K	CS21912FB13	0.95V
Bristol	3.16K	CS23162FB04	1.05V

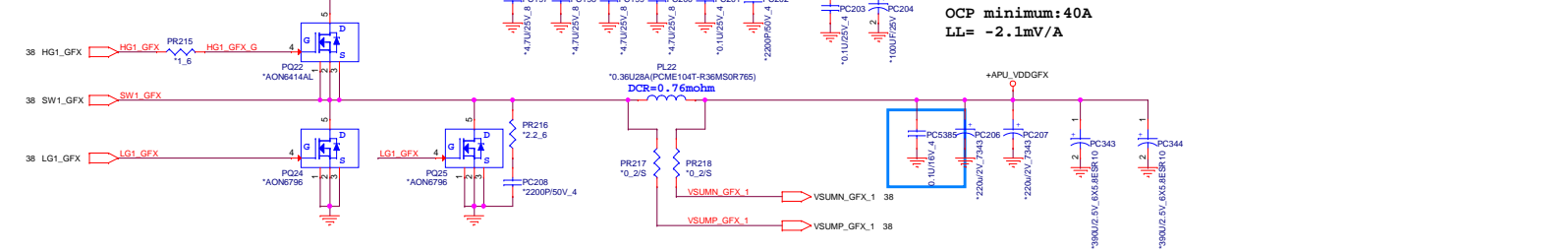
1.8VS5 +/- 3%
TDC: 3A
EDP: 4A

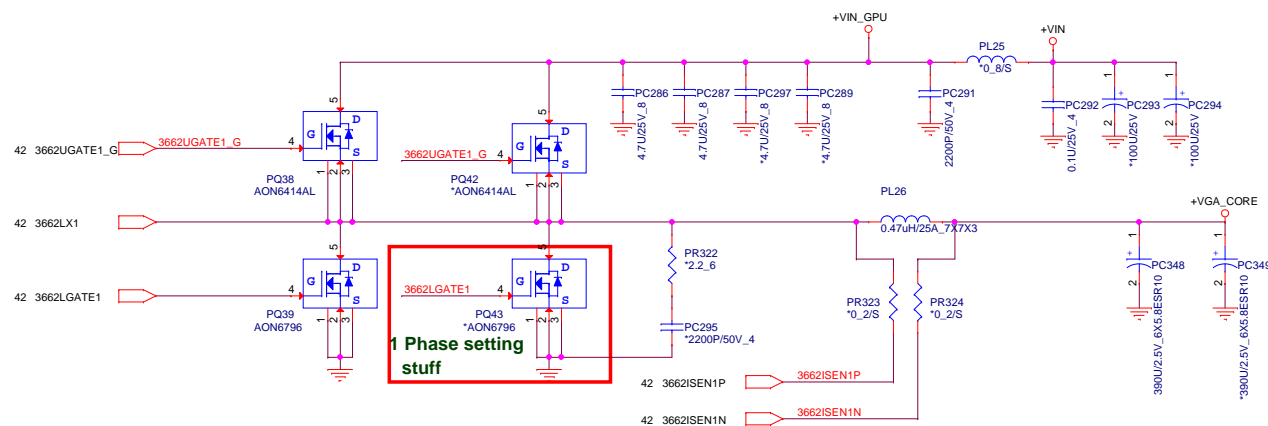




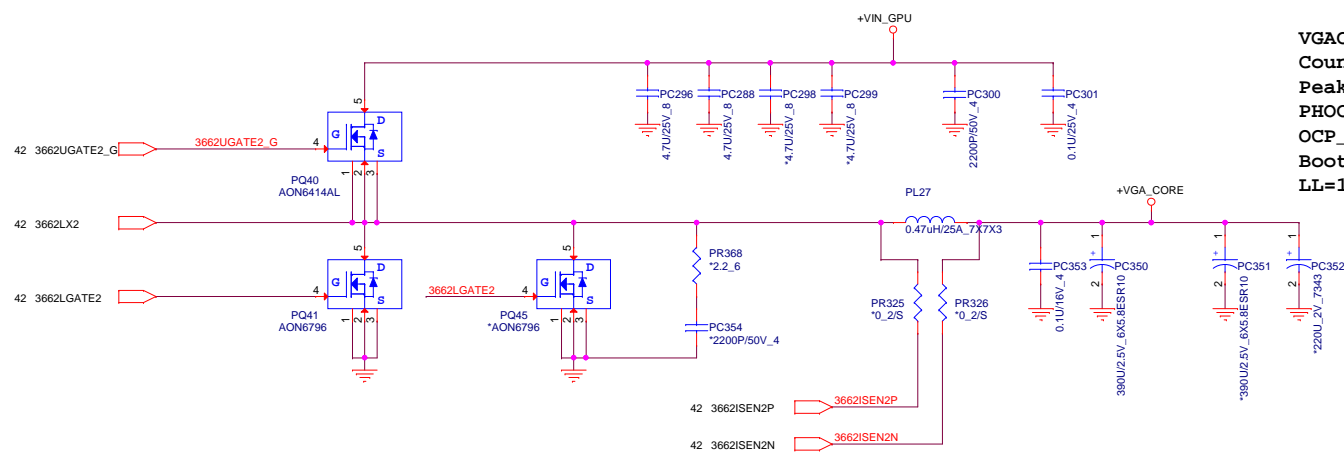
CPU	Page 38 & Page 39
Bristol	Stuff
Stonley	Unstuff







VGACORE (R16M-M1-70_ 25W/38W(1ms))
 Countinue current:28A
 Peak current=38A (1ms)
 PHOCP_TDC=40A (soft-start only)
 OCP_SPIKE=55A(1ms)
 Boot VID=0.9V
 LL=1m V/A

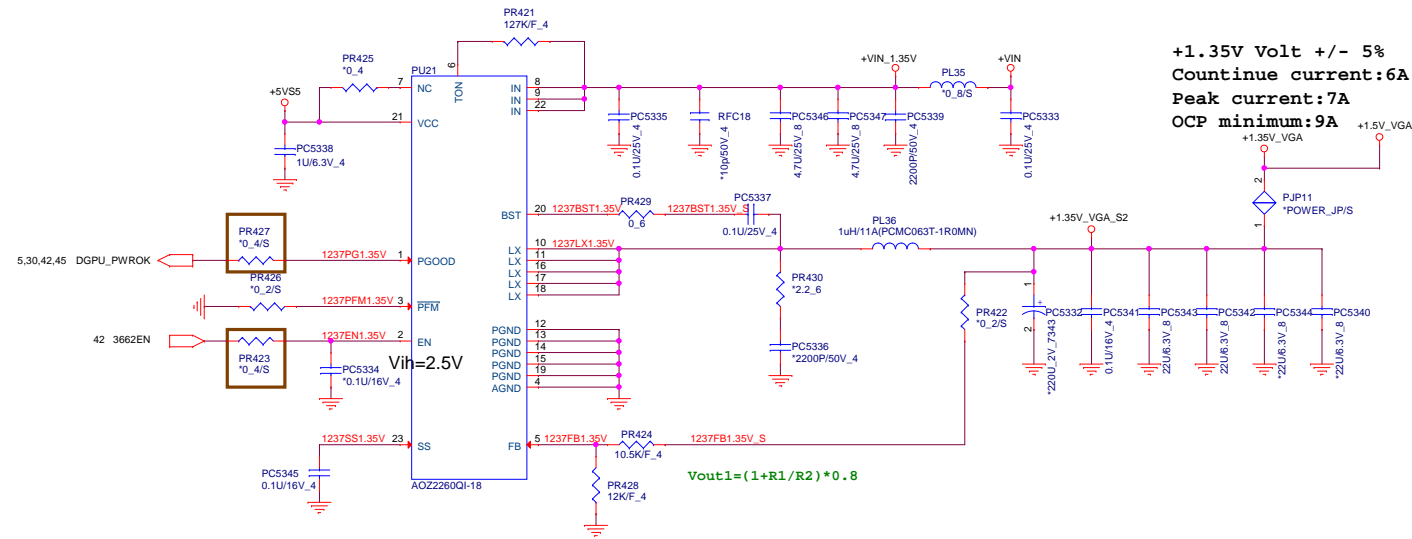


VGACORE (R16M-M2-50_ 37W/56W(1ms))
 Countinue current:40A (R16M-M2-50)
 Peak current:56A (1mS) (R16M-M2-50)
 PHOCP_TDC=40A
 OCP_SPIKE=75A(1ms)
 Boot VID=0.9V
 LL=1m V/A



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	VGACORE(RT3662EB2)	1A
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	+1.5V_VGA(AOZ1236)	1A
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